AFIT/GE/ENG/00M-04

INVESTIGATION OF $Ge_2Te_2Sb_5$ CHALCOGENIDE FILMS FOR USE AS AN ANALOG MEMORY

THESIS

Travis Frederick Blake
Captain, USAF

AFIT/GE/ENG/00M-04

Approved for public release; distribution unlimited

The views expressed in this thesis are those of the author and do not reflect the official policy or position of the United States Air Force, Department of Defense or the United States Government.

AFIT/GE/ENG/00M-04

INVESTIGATION OF $Ge_2Te_2Sb_5$ CHALCOGENIDE FILMS FOR USE AS AN ANALOG MEMORY

THESIS

Presented to the faculty of the Graduate School of Engineering and Management
of the Air Force Institute of Technology
In Partial Fulfillment of the
Requirements for the Degree of
Master of Science in Electrical Engineering

Travis F. Blake, B. Computer Engineering.
Captain, USAF

March 2000

AFIT/GE/ENG/00M-04

INVESTIGATION OF $Ge_2Te_2Sb_5$ CHALCOGENIDE FILMS FOR USE AS AN ANALOG MEMORY

Travis Frederick Blake, Bachelor of Computer Engineering
Captain, USAF

Approved:

Major Charles P. Brothers, Jr., Ph.D. Thesis Advisor	9 Mar 00 Date
Major James A. Lott, Ph.D. Committee Member	29 FEBRUARY 2000 Date
Major Richard A. Raines, Ph.D. Committee Member	8 Mar 00 Date
Dr. Harald Schöne Committee Member	March 1, 2000 Date

Acknowledgments

First, I would like to thank my thesis committee, Maj Lott, Maj Raines and Dr. Schöne for their patience and guidance throughout this process. I would especially like to extend an appreciation to Dr. Edwards for his taking the time to lend his knowledge and experience to helping me understand this subject. Finally, I would like to recognize my thesis advisor, Maj Brothers. The guidance and direction he supplied was invaluable in helping me reach the end of this enormous effort.

I would also like to thank the other AFIT students, especially Capt Vern Starman and Lt Jeremy Stinger, who shared in this wonderful experience. Their advice and laughter proved very helpful at some very discouraging times.

Lastly, and most importantly, I would like to thank my family. I thank my Mom and Dad for all the tremendous support they have given me for more than 25 years and my mother- and father-in-law who allowed me to escape school and relax on much needed vacations. The biggest thanks and appreciation goes out to my wife, Kelly, who graciously put up with all the time away from home and late nights without any complaints. I simply could not have done this without her support. Finally, to my children, Michael and Lauren, although you have just entered this world, the thought of you has always been with me to keep my priorities always in perspective and to keep my feet on the right path.

Table of Contents

List of Figures

List of Tables

Table Page

List of Equations

Abstract

This work investigates the feasibility of using $Ge_2Te_2Sb_5$ chalcogenide films for analog memory. Thick film chalcogenide memory devices provided by Ovonyx, Inc. are characterized to determine how well the devices meet the repeatability, stability and predictability criteria needed to accurately store analog data values. Chalcogenide memory devices take advantage of the phase-shifting nature of chalcogenide materials to store the analog data as a resistance level.

An automated test system was developed to characterize the material and the prototype devices with the goal to determine the 1) non-destructive readability of the device at different resistance values; 2) repeatability of programming the device; 3) stability the resistance value has over time; 4) parametric variations between devices; and 5) maximum and reliably achievable analog resolution.

The results of these characterizations demonstrate that thick film chalcogenide devices possess the necessary repeatability, stability and predictability properties needed in an analog memory, with at least a 4-bit analog resolution. However, the prototype devices, as produced for this research, do not demonstrate these properties consistently. A full scale, commercial fabrication process is likely to improve the device design and manufacture so it can be used as an analog memory.

INVESTIGATION OF $Ge_2Te_2Sb_5$ CHALCOGENIDE FILMS FOR USE AS AN ANALOG MEMORY

1. Introduction

1.1 Introduction

Many traditional applications, such as signal and image processing, and some emerging applications, such as artificial neural networks, will greatly benefit from a reliable, accurate memory that can store analog data values. Unlike their digital counterparts, analog memories have the ability to store a wide, ideally infinite range of data values in-between the traditional logical '1' and '0' levels. Therefore, analog memories have to be sensitive to a much wider range of programming levels than the binary values of digital memory. The wider the distance between the high and low programming levels of the analog memory, the more distinguishable, stable states the memory will have and the more precise analog data the memory can store.

1.2 Problem Statement

While many different analog memory structures exist, all of the current analog structures suffer from undesirable characteristics [1]. For example, some require programming voltages that are much higher than the circuit's operating voltage (>10V), while others suffer from data retention problems [1]. Still others are not compatible with current very large scale integration complementary metal-oxide-semiconductor (VLSI

CMOS) circuit processing and therefore make device integration into silicon circuits much more challenging [1].

The goal of this research is to investigate and document the ability of an amorphous semiconducting material known as chalcogenide to be used as an analog memory. The inherent characteristics of chalcogenide materials have the potential to make them a good choice for storing analog data values. Initial work on memory devices based on chalcogenide materials have shown reasonable programming voltages of approximately 1V to 2V, with fast programming times of less than 100ps, along with excellent value retention [2]. However, due to the phase-shifting nature of the chalcogenide material, repeated programming levels may not always result in the same stored data values [2].

1.3 Approach

Desirable attributes of analog memories, such as data retention and programming sensitivity, must be defined before investigating the suitability of chalcogenide devices for analog data storage. A review of the properties of chalcogenide will be presented and the material properties are reviewed to determine if chalcogenide devices can be effectively used as an analog memory device; i.e. none of the material properties conflict with the desired analog memory attributes. Finally, a suite of procedures to characterize the material will be developed to determine if the material meets these desired attributes.

1.4 Overview

This thesis is organized into six chapters beginning with an introduction to the research. The rest of the chapters progress in a logical flow, beginning with background information on both chalcogenide materials and analog memories, then moving on to a characterization approach, a characterization plan and the results and analysis of the measurements.

Chapter Two contains an overview of analog memories and chalcogenide materials. The overview also includes a discussion of the desirable characteristics of analog memories and a review of different analog memory structures. Additionally, an introduction to amorphous semiconductors and a discussion of the properties of chalcogenide materials is presented.

The characterization approach, presented in Chapter Three, introduces the scheme that is followed to characterize the chalcogenide memory devices. The characterization approach relies heavily upon the material properties and the desired analog memory attributes discussed in Chapter Two. The approach contains, in general terms, a philosophy about how to demonstrate that the chalcogenide material meets the analog memory properties needed for accurate analog data storage. The term characterization is used instead of test because there are no set of standard results to compare to the outcome of the experiments. So instead of testing the devices to see if the results meet established values, the results are used to *characterize* the behavior of the material.

The characterization plan presented in Chapter Four builds upon the characterization approach and states the purpose, a general description, and the actual procedure of each of the characterizations used to investigate the device. Included in the

characterization description are the expected results for each characterization, as based on preliminary data and knowledge about chalcogenide materials. The results and analysis of the characterizations conducted in this research are given in Chapter Five.

Chapter Six ends the thesis with conclusions and a comparison of the results with the desired analog memory characteristics discussed in Chapter Two, and expanded on in Chapter Three. Chapter Six also includes other relevant comments, lessons learned and recommendations for future research in this area.

2. *Literature Review*

2.1 Introduction

Over twenty years of study has been conducted in both the areas of chalcogenide materials and analog memory technology culminating in numerous articles and books. This chapter contains a brief overview of the work done in these fields, including the properties of chalcogenide materials and the types of analog memories.

2.2 Chalcogenide Materials

In the 1950s, Dr. S. Ovshinsky, interested in neurophysiology, began work to understand how nerve cells store, switch, alter, and transfer information in an organism [3]. In pursuit of this knowledge, he reported working with a class of materials that were thought to be rather uninteresting, with no exciting characteristics. This group of materials, known as amorphous semiconductors or noncrystalline solids, was thought by early researchers to behave like intrinsic semiconductors [3]. Since intrinsic semiconductors were common, new and exciting phenomena was not expected. In fact, these materials demonstrated a low Hall mobility and appeared to have very few free carriers that demonstrated little ability to move freely when induced by an electric field [3]. However, by 1968, Dr. Ovshinsky and others succeeded in creating two amorphous semiconducting devices utilizing chalcogenide materials that demonstrated anything but common behavior.

2.2.1 Characteristics and Physical Properties

Amorphous semiconductors can show some very unique characteristics. Unlike crystalline semiconductors such as silicon and germanium, amorphous semiconductors have a very limited long-range periodic order. The limited long-range periodic order allows amorphous semiconductors to have electrical and optical behaviors that are far different from their crystalline counterparts [4]. Chalcogenide materials are combinations of atoms that contain one or more Column VI elements, known as chalcogens, and other crosslinking elements. These compounds, such as As_2S_3, $Se_{55}As_{12}Ge_{33}$ and $Ge_{28}Sb_{12}Se_{60}$, form amorphous alloys with a wide variety of electrical properties depending on the exact chemical composition. A typical chalcogenide material compound is shown in Figure 1.

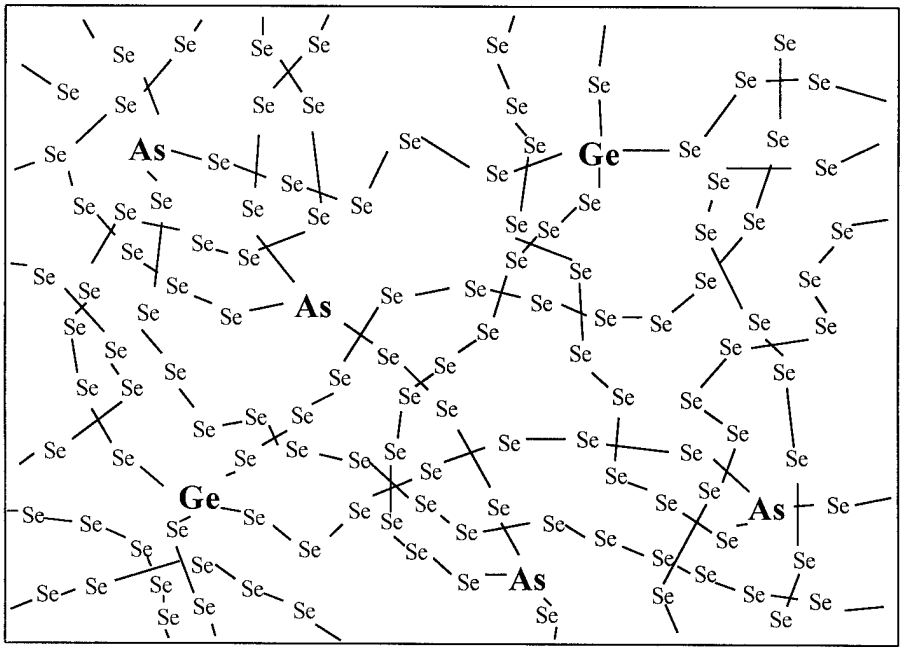


Figure 1. Schematic bonding topology of $Se_{1-x-y}As_xGe_y$ [5]

2.2.2 Electrical Conduction

Many amorphous semiconductors, including chalcogenide materials, demonstrate very little electrical conduction. While the exact cause for the limited conduction in chalcogenide is not completely understood, two theories have been put forward. The first theory is based on bonding defects within the structure of the material and has been widely publicized in the literature. While this theory does an adequate job in explaining most of the observed behavior in chalcogenide material, it falls short in describing the results of some newer experiments [6]. The second theory involves the creation of small polarons within the material. The small polaron theory is a simpler explanation for the behavior of chalcogenide materials and has gained increased interest in recent years [6]. Since the exact mechanisms for electrical conduction is not completely understood, and the defect theory has received most of the attention in published literature, it will be used to help explain some of the behavior seen in chalcogenide materials.

2.2.2.1 Defect Theory

In a perfect crystal, all of the outer shell electrons of a particular atom are involved with chemical bonds to the atom's nearest neighbors. In an amorphous material, the lack of a long-range periodic crystal structure leads many outer electrons unbonded with neighbor atoms. These vacant bonding sites of unpaired electrons are referred to as dangling bonds [5]. Chalcogenide materials are also known as "lone-pair" compounds because of the four outer electrons (p-orbital) of the Column IV element used for bonding, only two are involved in the chemical bonding of that atom [5]. Figure 2 shows the "lone-pair" electrons in a sample chalcogenide material. The creation of the

valence-alternating pairs (VAPs) and the three-center bonds (TCBs) shown in Figure 2 are discussed later in this section. In Figure 2, circles designate chalcogen atom (*Ch*); empty (full) circles mark lone-pair (non-bonding TCB) electrons; strait (dotted) lines signify covalent (three-center) bonds.

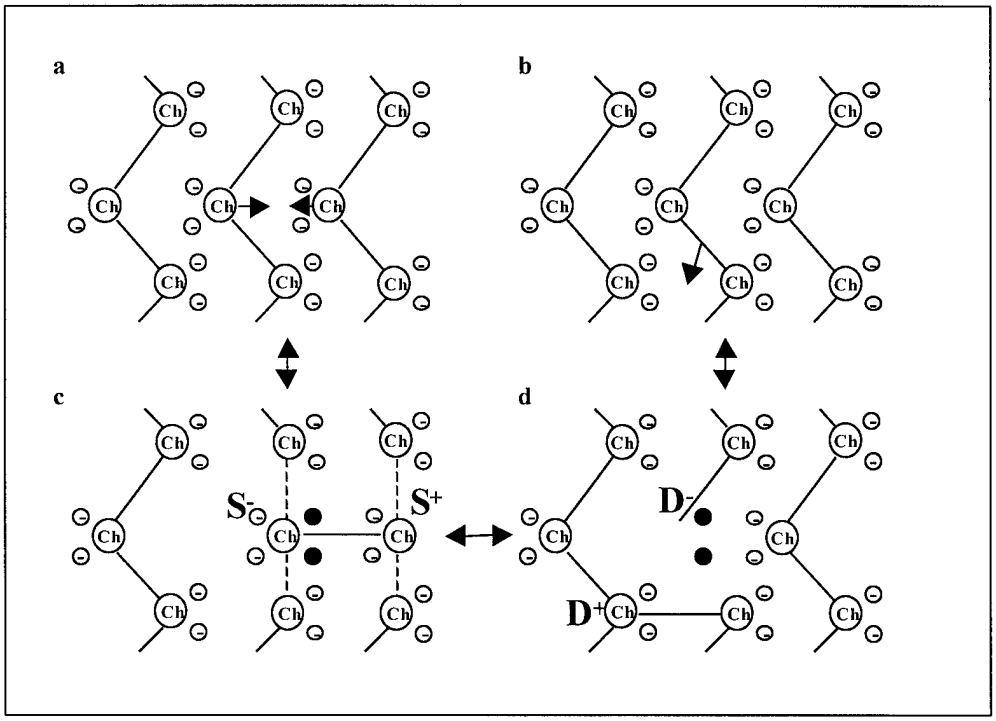


Figure 2. Sketch of TCB and VAP creation from [7]

In the defect theory, the key to comprehending the electrical behavior of chalcogenide is the understanding that it is the deviations from the normal bonding structure (NSB) of the alloy that controls electrical transport properties [5]. This condition is analogous to the deviations from perfect long-range order in crystalline materials controlling the crystalline material's electrical properties [5]. In crystalline semiconductors, with a periodic arrangement of atoms, the energy states available to an electron as it moves through a solid are continuously distributed over certain energy

ranges, called bands, but are excluded from other energy ranges, called gaps [4]. While it might seem that long-range periodicity is a requirement for bands and gaps, investigation of crystalline semiconductors at the melting point has revealed otherwise. At the melting point of a crystalline semiconductor, the long-range periodic order of the material disappears, but the electrical properties remain [4]. Because a crystalline semiconductor behaves electrically the same below the melting point as it does above the melting point, it must also have the same energy band structure above and below the melting point. Since energy bands and band gaps do not depend on the long-range order of the material, amorphous semiconductors will also have energy bands and band gap structures [4].

Electrons within the band gap will not be able to propagate though the material. Since electrical conduction depends upon electrons moving through a material, any electron that cannot propagate through the material lowers the electrical conduction of the material. Investigation of amorphous semiconductors has shown that the density of states drops off sharply at the edges of the energy bands [4]. The rapid reduction in the density of states at the energy band edges implies that the energy band structure can also be thought of as a mobility band structure [4]. Within the mobility band structure, electrons will be able to propagate through the material within the bands and will not propagate within the mobility gap.

In all amorphous semiconductors, there are a large number of states, or electron traps, within the gap of its mobility band structure. The states within the band gap are due to the large number of traps in the material created by dangling bonds and other non-periodic bonding defects within the material, called deviant electron configurations

(DECs) [5]. As described in [8] and [9] neutral dangling bonds containing unpaired electrons form a positive and a negative trap according to the configuration:

$$2Ch_3^0 \rightarrow Ch_3^+ + Ch_1^- \quad (1)$$

Where the *Ch* indicates a chalcogen element, the subscript denominates the coordination number of the atom (the number of bonding neighbors) and the superscript the charge of the trap. The reaction given in (1) is exothermic and therefore the creation of the valence-alternating pairs (VAP) Ch_3^+ and Ch_1^- are preferred over the neutral Ch_3^0 since it lowers the energy of the system [8,9]. In addition to the VAPs, there has also been some recent evidence for states shallower than the VAPs. These shallower states, called three-center bonds (TCB), are formed from other structural deviations [7].

The VAP or TCB traps, form states in the gap of the mobility band structure of the material. The gap states trap electrons and holes by ionic attraction within the gap causing the lifetimes of the carriers in chalcogenide materials to be dramatically reduced when compared to crystalline materials. The reduction in the carrier lifetimes lowers the mobility of the carriers, which in turn decreases the conductance of the chalcogenide materials. Since the reciprocal of the conductance is the resistance of the material, a reduction in the mobility within the material also increases its resistance. To control the electronic properties, i.e. the electrical conduction, of chalcogenide materials, additional elements must be included to add or remove the states in the mobility gap [5]. To increase the resistance of a chalcogenide material, elements that cause the material to form more bonding deviations and, therefore, more traps within the mobility gap, should be added. To decrease the resistance, elements that prevent dangling bonds should be added to the chalcogenide material. The elements that reduce the number of dangling

bonds will reduce the number of traps in the mobility gap and will increase the electron's mobility through the material.

2.2.2.2 Small Polaron Theory

The small polaron theory speculates that electrical conduction in chalcogenide materials is reduced by the formation of "self-induced" electron traps [10]. A small polaron formation in a sample crystalline structure is shown in Figure 3.

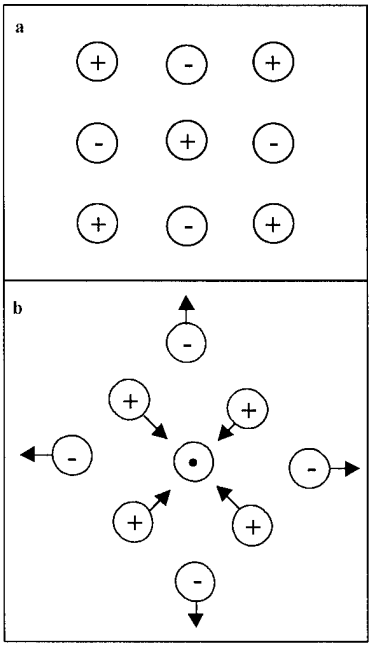


Figure 3. Small polaron formation in a crystal from [10]

Figure 3a shows a regular two-dimensional ionic lattice structure. When an electron in added to the system and is stationary in the site of the positive ion, the electron will tend to displace the surrounding atoms, as shown in Figure 3b [10]. The displacement of the atoms forms a "self-induced" potential well that could be sufficiently deep to prevent the electron from moving through the material [10]. Unless the

surrounding atoms are altered to remove the potential well, the electron will remained trapped at this site [10]. This situation is energetically stable if the increase in the strain energy associated with the displacement of the atoms is smaller than the decrease in the energy of the electron due to its binding in a self-induced well [10]. While Figure 3 depicts the formation of a small polaron in a crystal, there is no need for a periodic arrangement of atoms to allow the formation of the self-induced well. Indeed, the non-periodic nature of amorphous semiconductors could aid in the formation of small polarons. The disorder in the amorphous material slows down electrons, localizing the electrons at an atomic site long enough displace neighboring atoms and form the self-induced potential well [11]. Electrical conduction in the small polaron theory occurs via polaron hopping. A formed polaron can propagate through the material by hopping to an energetically identical atomic site [10]. By hopping to several sites, an electron can move though a material in a polaron, then be freed from the potential well when the structure of the surrounding atoms are altered near the edge of the material.

2.2.3 Phase-Shifting in Chalcogenide

The distinguishing characteristic of chalcogenide materials is the material's ability to transition between an amorphous and poly-crystalline structure. While not all compositions of chalcogenide materials exhibit this behavior, given the correct cross-linking atoms (such as Ge and Sb), the structure of the material can be switched between the pseudobinary line shown in Figure 4.

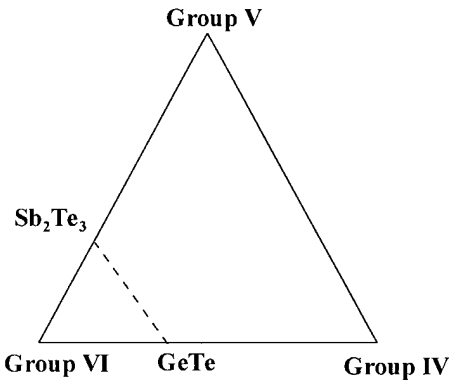


Figure 4. Pseudobinary line for possible phase change materials from [2]

The phase-shifting behavior in this type of chalcogenide material, known as a bistable material, is accompanied by a change in the atom structure of the material. While the exact nature of the structural change within the material is unknown, the phase-shifting is thought to involve a combination of electrical and thermal processes [12]. Given a selection of bistable chalcogenide with an amorphous structure, thermal energy supplied to the material will allow the atoms of the material to break the bonds between neighboring atoms [12]. Once the atoms are unbonded, they are free to align in a poly-crystalline structure. The atoms will tend toward a poly-crystalline arrangement since this arrangement has a lower energy than the amorphous structure [12]. The amount of poly-crystallinity induced into the bistable material is dependent how the long the energy is supplied to the material and how the energy is removed from the material. The longer the bistable material is supplied with an energy above the energy barriers for bond breaking, the more time the atoms in the material will be allowed to move into a poly-crystalline structure [12]. The transition from amorphous to poly-crystalline is shown in Figure 5.

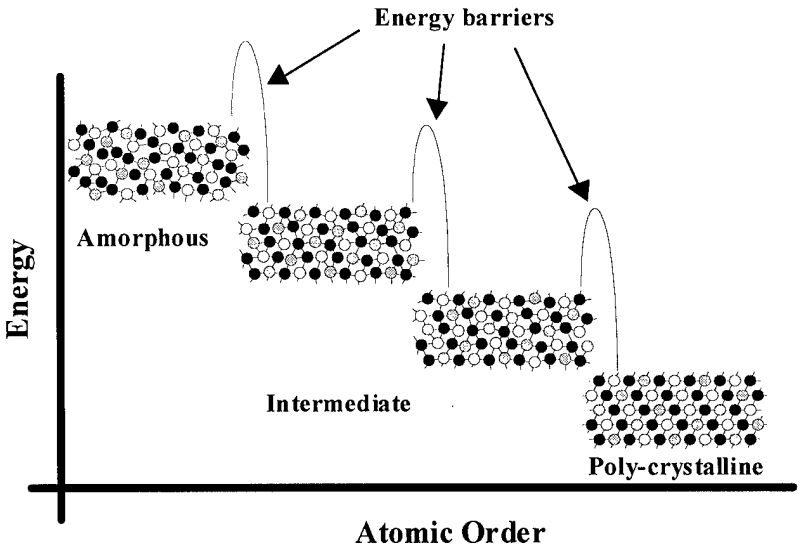


Figure 5. Thermally induced phase-transition in bistable chalcogenide from [2]

As Figure 5 shows, intermediate states exist between the amorphous and poly-crystalline structures. These states occur when the energy supplied to the material is not sufficient to allow all the bonding of neighbor atoms to break and realign. Instead, only part of the atoms are allowed to align, leading to partially amorphous and partially poly-crystalline structures.

Once in a poly-crystalline state, the bistable material can be transitioned back into an amorphous structure by again supplying thermal energy [12]. As soon as the energy breaks the bonds of the atoms in the material, or "melts" the material, the energy is rapidly removed (known as "quenching") to lock-in the random arrangement of material bonds by returning the "melted" material to a solid state. The energy to return the material to an amorphous structure must be high enough to allow for the bonds of the material to be broken, but the length should be short enough to prevent the atoms from being able to align back into a poly-crystalline state.

There are also intermediate states between the mostly poly-crystalline and completely amorphous structures of the bistable material. Although the reason for these intermediate partial amorphous, partial poly-crystalline structures is not completely understood, they maybe caused when the atoms of the material are placed in "meta-stable" states [13]. The energy supplied to the atoms of the bistable material not only allows the atoms to break bonds with neighboring atoms, but also can excite the atoms [13]. The amount of excitation imparted to the atoms is dependent of the amount and time that the energy is supplied to the material. Atoms in excited or "meta-stable" states are too energetic to align in a low energy crystalline arrangement [13]. Therefore, the structure of the material is placed in a mixture of amorphous and poly-crystalline alignment.

The bistable chalcogenide material is one of two compositions of chalcogenide alloys that can be useful in forming electronic devices.

2.2.4 Chalcogenide Switching Devices

Elements can be added to chalcogenide materials to form two fundamentally different types of chalcogenide devices. The additional elements act as crosslinks between the chalcogen atoms, controlling the density of localized states within the gap [14]. The control is accomplished by dictating the amount of crystallization allowed in the amorphous material. Any amorphous semiconductor has local periodic order, but a limited long-range periodic order. However, the amount of long-range periodicity, or crystallinity, can vary dramatically from one amorphous material to another. By adding the appropriate crosslinking atoms, an amorphous material can be pushed toward, or

restricted from, a more crystalline state [14]. An amorphous semiconductor with a higher crystallinity than another will have fewer dangling bonds and thus fewer states within its mobility gap.

Atoms that form strong bonds and crosslinks are added to the chalcogenide alloys to increase the number of gap states in the material. Dopant atoms, such as silicon, germanium or arsenic, frustrate crystallization by stertic hindrances [14]. These doping atoms bond strongly to the elements of the alloy in a highly amorphous state leading to a large density of lone-pair electrons and states in the mobility gap.

Just as certain elements can be added to chalcogenide alloys to increase the density of states in the mobility gap, others can be added to reduce these states. Atoms such as antimony, tin and lead can be used to form weak bonds and crosslinks [14]. Weak bonds allow a higher level of crystallinity and thus fewer gap states. With fewer states in the mobility gap, electrons moving through the material encounter fewer obstacles and have a much higher electrical conduction.

The type of chalcogenide alloy that utilizes a large number of states in the mobility gap and strong crosslinks is referred to as an unistable material and is used to produce a threshold switch. The other material type with weaker crosslinking atoms is a bistable material (discussed in section 2.2.3) and is used in the production of a memory switch [14].

2.2.4.1 Threshold Switch

The threshold switch is a device that has a high impedance at a low voltage that can be rapidly switched to a high conductance state when a threshold voltage, V_{th}, is

reached [15]. The device remains in this high conductance state while a minimum holding current, I_h, is maintained. As soon as the current falls below the holding current, the device is rapidly switched back to a high impedance state [15]. The basic I-V characteristic of this device is given in Figure 6. The switching time, t_s, for the high impedance to high conductance states and vice versa has been reported to be less than 100ps for a given chalcogenide material composition and device structure [16]. The level of the threshold voltage is dependent on the specific amount and type of crosslinked elements added to the chalcogenide alloy and can be set to be anywhere from a few volts to over 300V [15]. The resistance values measured in the high impedance state can be as high as several Mega-Ohms, while those in the conducting state can be less than one Ohm [15].

Although the exact switching mechanism for the threshold switch is not exactly known, it is thought to involve an electrical process that fills the states in the mobility gap of the material [17]. The threshold switch formed from an unistable chalcogenide alloy, such as $Te_{39}As_{36}Si_{17}Ge_7P_1$, has a very high density of states in the gap, and therefore normally has a very low conductance. When the voltage across the device is increased, carriers created by the applied electric field near the electrodes begin to fill the numerous gap states. When these gap states are filled, there are suddenly few hindrances to the mobility of the carriers [17]. At this point, the conductance of the device increases rapidly and the device is switched into the high conductance or "on" state. As long as a minimum current is maintained, the states in the gap will remain filled and the conduction of the material will remain high. As soon as the current falls below the holding current, electrons no longer fill the gap states. Gap states begin to severally

hamper electron mobility and the device rapidly returns to a high impedance or "off" state. Since the threshold switch requires a holding current to maintain the high conduction state, it is a volatile device. Another chalcogenide device that is independent of a holding current is the nonvolatile memory switch.

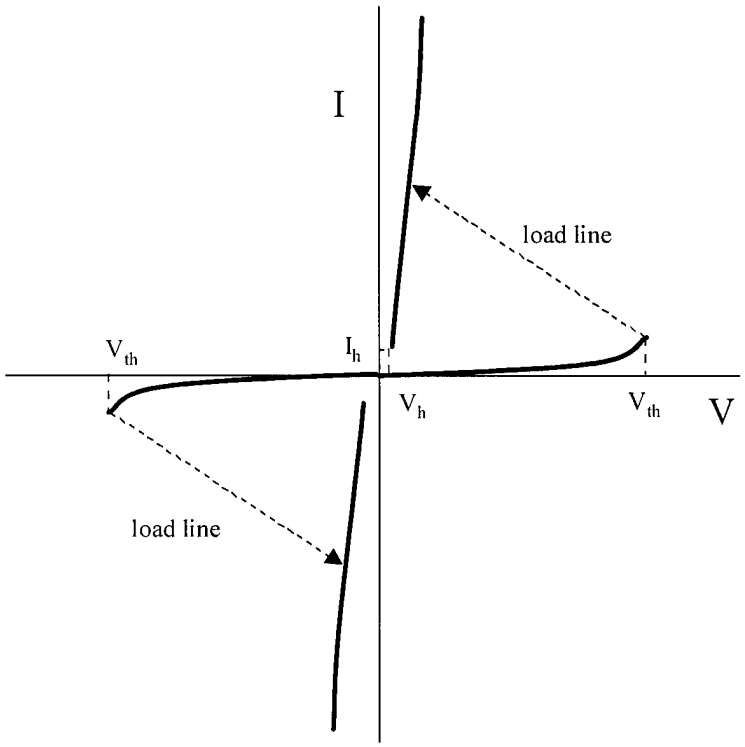


Figure 6. I-V Characteristic of a Threshold Switch [15]

2.2.4.2 Memory Switch

The memory switch is a device that is able to hold a high or low conduction value even in the absence of any type of holding current or voltage, and therefore can be used to store a set conduction level. The memory switch uses a bistable chalcogenide that allows a change in the conduction of the device to be held even in the absence of a

current or voltage [11]. As shown in Figure 7, a memory switch with the bistable material shows I-V characteristics that are very similar to those of the threshold switch. However, the curve for the memory switch continues through the origin of the graph showing that, once in a low impedance state, a holding current or voltage is not required. The nonvolatility inherent in the bistable chalcogenide material can lead an attractive memory device.

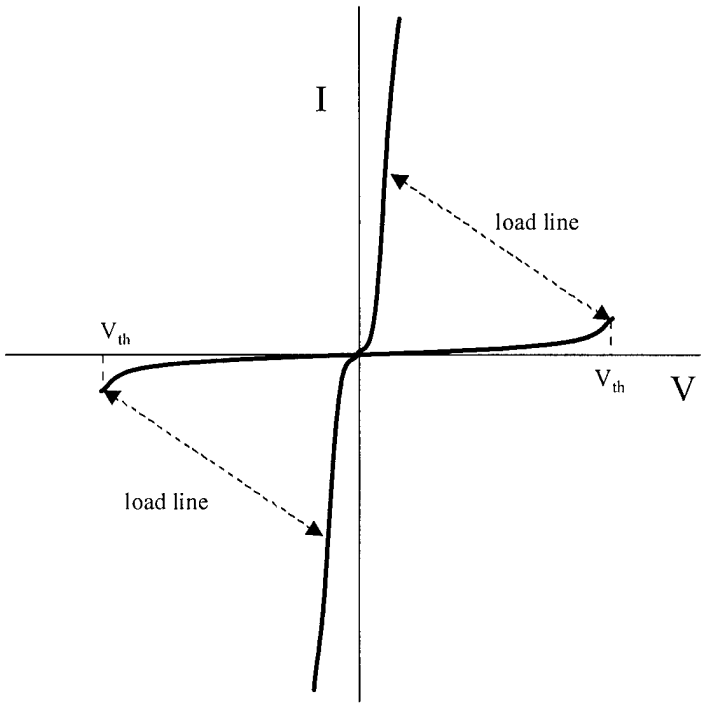


Figure 7. I-V Characteristics of a Memory Switch [11]

The memory switch consists of a bistable chalcogenide alloy between two metallic electrodes. A graphical representation of the set and reset process in a bistable chalcogenide memory device is given in Figure 8.

Thermal energy is supplied to the material in the form of a current/voltage pulse through the electrodes. The transition of the material from a highly amorphous (high

resistance) structure to a poly-crystalline (low-resistance) structure is accomplished according to the description in section 2.2.3, by forming a crystalline filament between the electrodes. The filament is created towards the center of the device where the energy is the greatest [11]. Areas of the material outside of the crystalline filament remain in an amorphous state. [11]. A current pulse with a long duration is supplied to the bistable material to transition it to a poly-crystalline state, while a pulse with a high amplitude and short duration is used to place the material back into an amorphous structure, removing the formed crystalline filament [11]. The switching times of bistable material are on the same order (<100ps) as the threshold device [15].

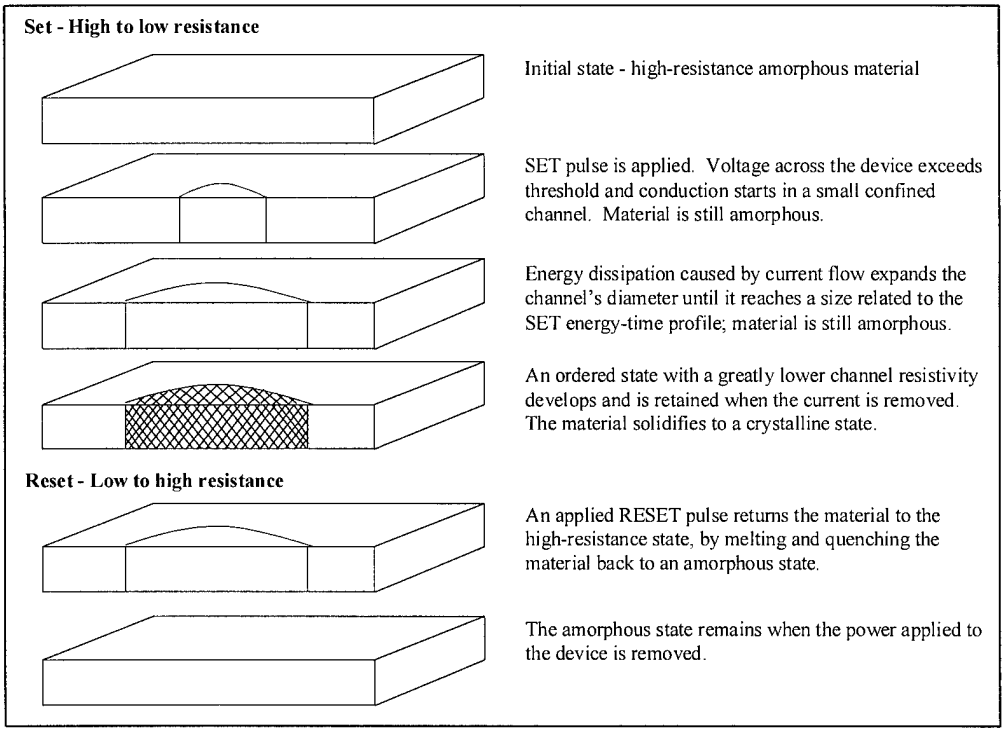


Figure 8. Schematic of switching in a chalcogenide memory device from [18]

2.2.5 Summary of Chalcogenide Materials

Although initially thought to be uninteresting, amorphous semiconductors have shown themselves to have some very unique properties. Research into these materials has shown that controlling the density of states in the energy band gap is the key to using these materials to form useful electronic devices. In particular, chalcogenide alloys, when combined with different crosslinking atoms, can exhibit some very interesting electrical properties. Strongly and weakly bonded atoms can be added to chalcogenide alloys to form unistable and bistable chalcogenide materials. These materials can then be used to produce two classes of switching devices: the threshold switch, which keeps its amorphous state throughout its operation, and the memory switch, which is able to switch between high and low amorphous states. A thin film chalcogenide memory switch has already proven itself as a non-volatile digital memory [14]. An derivative of this device, the thick film chalcogenide memory switch, could prove itself as a highly successful analog memory.

2.3 Analog Memory

Ideal analog memories are designed to store any data value between their absolute maximum and minimum programmable values. This is in contrast to digital memories, which only store binary data values (i.e. logical 1's and 0's).

The technological push in recent years has been to convert electronic applications to a digital format [20]. Most of the data brought into an application, especially from the outside world, is analog in its origin. To allow this analog data to be used in a digital system, it must first be converted to a digital representation by an Analog-to-Digital

converter (ADC). For data such as the unsigned integer 45_{10}, this is easily done and results in the 8-bit binary number 00101101_2. For other data, such as decimal numbers with hundreds of digits, the resulting binary number maybe hundreds or thousands of bits long, requiring large amounts of digital data storage. Furthermore, the conversion from analog to digital data is time consuming and in most applications severely limits the data throughput. It adds latency to time critical applications and in most case results in a loss of data fidelity. Once the analog data is converted into a digital format, most applications require the data to be stored in digital memory were a single bit occupies a single memory cell. An analog memory can virtually eliminate the conventional costly, time consuming and, at times, resolution degrading digital to analog conversion step that is necessary for all image processing and many sensory input analysis applications.

For most applications, a digital system has the advantage of no data degradation during further processing and can be less susceptible to noise or other environmental factors than an analog system [20]. However, for some specific applications, such as neural networks, an analog format can prove to be 10^6 times faster than digital systems [20]. The speed-up is due in-part to the fact that the analog system does not have to perform the analog-to-digital conversion necessary for a digital system. Also, unlike digital systems that are usually synchronized to the rising and falling edges of a controlling clock, analog systems, such as the Hopfield algorithm, can run continually in a complex feedback circuit. Asynchronous analog systems can allow the analog system to complete optimizing operations in less than one digital clock cycle, where as the synchronous digital system may require 100,000 or more clock cycles to complete [20].

Additionally, analog systems can also have a potential accuracy advantage over digital systems. In order to maintain a high processing speed with a lower power consumption, digital conversion of analog data must be limited to a set number of bits, such as 32, 64 or 256 [20]. This limitation may mean, especially for large decimal numbers, that the digital conversion introduces an error into the data value since it does not have the full number of bits necessary to accurately store the data value. Therefore, the analog system can operate on a more precise value than the digital system [20].

A memory is needed to store analog data values in order for these analog systems to operate. Analog memories are specifically designed to store the analog information in one device, rather than the closest digital representation of the data in many digital memory devices.

Additionally, analog memories can also be useful in digital systems where bits stored in many digital memory devices can be combined and stored in one analog memory device. For example, the bits of a 32-bit word can be weighted and added together (similar to a Digital-to-Analog conversion) to result in a unique value which could then be stored in a analog device. This 32-bit word can then be read out of the analog memory and converted back to a digital format using an ADC. This multi-bit per device storage could lead to the development of ultra-high density digital data storage.

2.3.1 Properties of Analog Memories

Since analog memories have the potential of allowing fast analog circuits and high-digital data density in digital systems it is not surprising that such devices have been developed. Before discussing the different types of analog memories, it is first useful to

define the desirable properties of an "ideal" analog memory. The characteristics of different analog memories can be compared and evaluated against an "ideal" analog memory device to determine which analog memories demonstrate better performance.

The key property of an analog memory is its ability to store analog data values between the high and low data levels. The memory must have sufficient programming sensitivity, allowing small changes in programming levels to correspond to small changes in the stored value. This ability to store a range of data values is the main difference between analog and digital memories. Though it is difficult to achieve, an ideal analog memory would have a unique data value for each programming level, i.e. every analog value is distinguishable from another. A good analog memory device should come as close to this ideal analog performance as possible.

Analog memory devices should also be easily programmable with reasonable programming levels. For example, if voltages are used to program a memory device with a certain analog value, then the voltages should not be extreme. Ideally, the programming voltage would be on the same order as the operating voltages of the circuit and would be scalable. Therefore, as the circuit using the memory was reduced in size requiring a lower operating voltage, the programming voltage for the memory device would also decrease [21].

Analog memories must retain the data stored in them. Additionally, the memory devices should also be insensitive to environmental changes. Differences in environmental variables such as temperature or radiation level should not change the values of the data stored on a device.

The memory devices should be accompanied by the minimum amount of support circuitry. Ideally, no additional circuits, such as voltage amplifiers, would be needed to program or read the memory devices. This implies that a simple relation between programming signal and analog storage values exists. Additionally, reading the stored data value should be non-destructive so re-write after read circuits would not be required. The minimum amount of support circuitry allows for simpler designs that are cheaper to produce and provide a much higher device density by allowing more die area for memory devices [21].

The analog memory devices should be CMOS compatible with easy integration to current production lines. No mater how capable the memory, if the cost to integrate the device into analog circuits is greater than the expected return profit from the memory devices, the memories will not be produced [21].

Five desirable properties of analog memories have been discussed in this section. The next section will provide a review of current analog memories to determine how they compare to these desirable memory properties.

2.3.2 Types of Analog Memory Devices

Analog memory devices are available in a wide variety of forms, from devices that have been traditionally used for nonvolatile digital data storage to ferroelectric capacitors [1]. While all of the analog memories presented in this section use a programming voltage to program data values, the structures of the memory devices are different. Despite the structural differences of these memories, the programming methods fundamentally change the same property of the device, the conductance. By

varying the conductance of each device, each memory cell can be programmed with an analog data value. Since the conductance is the reciprocal of the resistance, programming also has the affect of changing the resistance of a device. To read the stored data value for a memory cell, a known reading voltage is applied to one end of the device. The variable amount of current passing through the programmed resistance of the device is then detected with sense amplifiers at the other end.

2.3.2.1 Floating-gate

The first type of analog memory device is based on to the traditional floating-gate electrically erasable programmable read only memory (EEPROM) device [1]. As shown in Figure 9, this device operates by storing charge on an isolated gate added to a typical n-channel metal-oxide-semiconductor (nMOS) transistor. The gate is electrically isolated between two layers of silicon dioxide (SiO_2) and, because of the dielectric isolation, retains all of the charge stored on it. The amount of charge stored on this gate varies the voltage at which the nMOS transistor turns on (known as the threshold voltage of the nMOS transistor), which in turn varies the conductance of the channel.

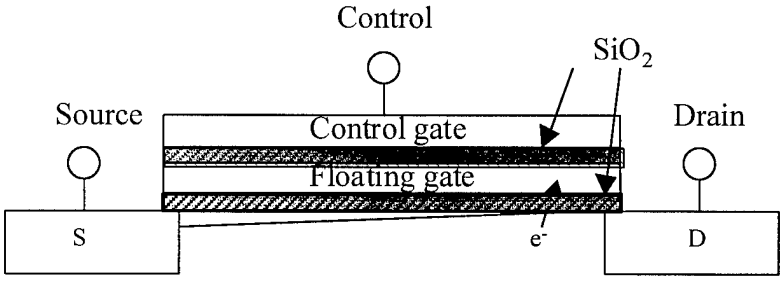


Figure 9. Floating-gate EEPROM analog memory device [22]

A large, positive voltage applied to the control and the source gates programs floating-gate memory devices. This voltage allows electrons to tunnel from the channel through the thin oxide under the floating-gate via Fowler-Nordheim tunneling and collect on the floating-gate [22]. The data stored on the device is read by applying a voltage to the source and the control gates [22]. If there is no charge stored on the floating-gate, then the voltage applied to the control gate will be coupled through the floating-gate and the channel of the nMOS transistor will invert. Inverting the channel allows current created by the voltage on the source to flow from the source to the drain. Conversely, if there is a significant amount of negative charge stored on the floating-gate, then the voltage on the control gate is not strong enough to overcome the opposite charge on the floating-gate and the channel is not inverted. Since the channel is not inverted, there is no conduction path from source to drain and no current flows in the device. For digital memories, the maximum amount of electrons possible are tunneled to the floating-gate during programming [22]. This large amount of charge on the floating-gate ensures the device has the "on-off" type of operation described above. For analog purposes, the programming voltage on the control gate can be varied so a variable amount of charge is stored on the floating-gate. When the read voltages are applied to the control and the source gates, the amount of charge on the floating-gate will then vary the amount that the channel is inverted. Since the channel is not fully inverted a variable amount of current will flow through the channel. Therefore, the amount of current that flows through the channel is directly controlled by the amount of charge programmed on the floating-gate. Since a different range of programming voltage values can be used to tunnel different

amounts of charge onto the floating-gate during programming, storage of analog data is possible [1].

Programming these devices requires high voltages (>10V) and programming is slow, usually in the millisecond range. However, an analog precision of 4-bits has been reported [1]. If the devices are produced with a high-quality oxide, these devices can show good data retention of greater than 10 years. Since the floating-gate device is fabricated in a standard CMOS process, integration into VLSI circuitry is not a complicated issue [1].

The floating-gate EEPROM can be used to store analog values by applying a variable voltage to the control gate. A similar nonvolatile memory can also be used in the same manner.

2.3.2.2 Charge-trapping

Charge-trapping devices are very similar to floating-gate devices. The main difference is the charge-trapping device uses a dielectric, such as silicon nitride (Si_3N_4), to store charge instead of the floating gate of the floating-gate device. Figure 10 shows a typical charge-trapping memory device.

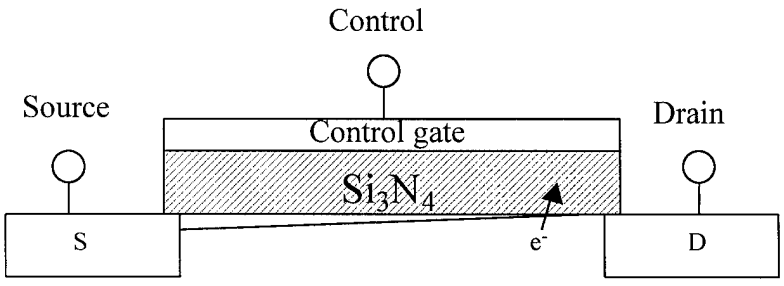


Figure 10. Charge-trapping analog memory device [23]

During programming, a large positive voltage placed on the control gate sets up an electric field between the control gate and the bulk material under the control gate. This electric field forces electrons to travel into the nitride where a large amount number of electrons are trapped in defect centers within the nitride. Just as with charge on the floating-gate, the trapped electrons change the threshold voltage of the n-channel transistor [23]. By varying the voltage on the control gate during programming, different levels of charge can be trapped in the nitride. The amount of charge that is trapped in the nitride leads to a level of channel inversion when the device is read. The amount that the channel inverts then leads to a observed device conductance. Just as with the floating-gate device, analog data storage is possible [1].

The charge-trapping device, like the floating-gate device, requires high programming voltages (>10V) and has a good programming sensitivity with 4-bits of precision reported [1]. Because of the extra fabrication steps of additional masks and deposition steps for the additional dielectric layers, charge-trapping devices are slightly more difficult to fabricate than the floating-gate devices [24].

The use of a dielectric is another way to store a variable amount of electric charge to allow the storage of analog data values. While floating-gate and charge-trapping analog memory devices are based on conventional binary nonvolatile memory, the next two examples of analog memories represent different approaches.

2.3.2.3 Ferroelectric

Ferroelectric materials are manufactured as dielectric films that polarize with the application of an electric field and remain polarized after the field is removed [23]. Different electric field strengths are used to induce various amounts of polarization in a ferroelectric capacitor, allowing analog values to be stored on the capacitor [1].

While ferroelectric memory devices are promising, these devices have not been as widely used as the floating-gate or charge-trapping memory devices. Programming ferroelectric materials can be accomplished with relatively low voltages (<1V) [1]. However, the polarization change during programming is usually extremely small so ultra-sensitive amplifiers are required to read the devices [25]. For a typical ferroelectric capacitor with a $10\mu C/cm^2$ range between the high and low polarization levels, this corresponds to just $0.625\mu C/cm^2$ for 4-bit precision. Reading the charge of ferroelectric capacitors typically is destructive since the capacitor must be de-polarized to determine the amount of charge stored on it. Additional support circuits are required to rewrite the initial information. Furthermore, the capacitors suffer from data retention problems [1]. The type of materials used to form the ferroelectric thin films makes them difficult to integrate into a CMOS fabrication process [25].

The extremely small changes in polarization that must be sensed to allow ferroelectric capacitors to store analog data values make these capacitors a difficult technology to use. Another analog memory provides a different storage possibility.

2.3.2.4 Amorphous Silicon (α-Si)

Another type of analog memory utilizes the characteristics of amorphous silicon. Unlike crystalline silicon that is used for the vast majority of microelectronic devices in use today, amorphous silicon has a large number of unpaired, dangling bonds [26]. These dangling bonds severally inhibit current conduction through the material by acting as carrier traps. The trapping of carriers by the dangling bonds dramatically reduces the mobility of carriers and therefore the electrical conduction of the material. The low conduction condition can be overcome by introducing an element such as hydrogen into the material through diffusion or ion implantation with high temperature annealing [24]. Hydrogen allows the dangling bonds of the amorphous silicon to be filled, reducing the number of traps and increasing the mobility.

The amorphous silicon device has a simple structure as shown in Figure 11. The amorphous silicon material is placed between two metallic electrodes and programming voltage pulses are used to vary the resistance of the material. By using selected metals for the device electrodes (such as vanadium (V) and chromium (Cr)), these devices have been shown to have a relatively large programming range of approximately 1.5V [1]. Programming amorphous silicon (α-Si) analog memory devices is achieved by applying a negative voltage pulse to write (lowering the device resistance) and a positive pulse to erase (increasing the device resistance) the stored information. Programming pulses are typically between 2V and 5V and are approximately 120ns in length [1]. Characterizations of amorphous silicon memory devices demonstrated the 2-5 V programming window was enough to program the devices with an accuracy of 5% in a range of 1kΩ to 1MΩ [1]. The exact programming mechanism for the amorphous silicon

memory device is not completely understood. However, the programming is believed to involve the diffusion of the metallic electrodes into the α-Si:H material along a filament less than 1μm in diameter [1,26,27]. The diffusion of the metallic electrodes leads to a dispersion of metallic atoms in the insulating α-Si:H material increasing its conductance along the formed filament. The filament can be removed by applying the programming pulse of reverse polarity. The reversed polarity removes the dispersed metallic atoms, removing the current filament and returning the device to its highly resistive state [1]. The formation of the filament is non-volatile and has been found to be tolerant to both temperature and radiation induced stress [26].

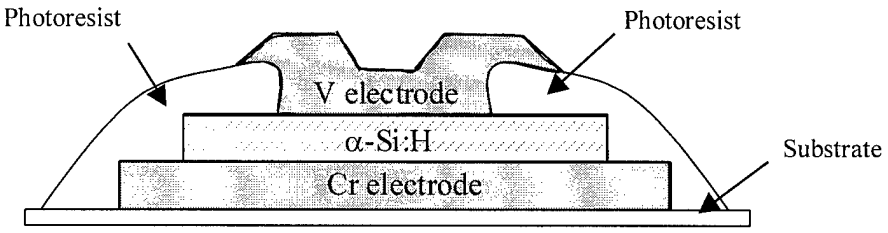


Figure 11. α-Si:H Analog Memory Device [1]

While the programming voltages of these devices are reasonable and on the same order of duration as the chalcogenide devices, the necessity of using both positive and negative voltages adds additional programming and implementation complications [1].

2.3.2.5 Summary of Analog Memories

Different approaches to create useful and affordable memory devices have been reviewed. The devices reviewed range from the commonly used floating-gate and charge-trapping EEPROM to the more exotic ferroelectric capacitor and devices using

amorphous silicon. While all of these devices have demonstrated some qualities that make them an adequate analog memory, they all have drawbacks. Programming times in excess of a millisecond, short retention times, high programming voltages and incompatibility with CMOS processing are all short-comings that need to be eliminated to form a more efficient analog memory.

2.4 Literature Review Summary

While all of the analog memory devices presented in section 2.3 provide potential solutions for analog memories, they all have some properties that are not desirable. Chalcogenide memory devices, which have already proven themselves in a nonvolatile digital memory role, maybe able to come closer to achieving all of the desired characteristics of an accurate, reliable and easy to produce and use analog memory [14].

The chalcogenide material and memory devices still require extensive characterization to validate them as a viable approach to achieving an accurate, affordable and highly reliable analog memory. The previous chapters served to outline the current memory approaches and their respective shortcomings. The next section will refine the properties of an ideal memory into verifiable metrics and will outline an experimental approach to test the chalcogenide memory devices for the compliance with these metrics.

3. Characterization Approach

3.1 Introduction

The ability to program the chalcogenide memory device to varying resistance levels may make the device suitable to store analog data values. To investigate the chalcogenide memory device's viability as an analog memory, a characterization approach must be developed. Building this approach first requires the desired properties of analog memories to be reviewed and those properties that the material must meet have to be determined.

3.2 Material Properties of Analog Memories

The material properties of analog memories discussed in section 2.3.1 can be divided into two broad categories. The first category includes all the properties associated with programming the device. These programming properties include the desire for low programming voltages, fast programming times and no additional support circuitry. These properties are set by the composition of the chalcogenide material and the structure and size of the memory device, and do not normally change for memory devices with a given material composition.

The second category of analog memory properties are dependent on the deposited material and can be subject to wide scale variation even between devices manufactured in the same array. The deposited material properties include the sensitivity to different programming pulses and insensitivity to external influences such as temperature. These

analog material properties can be broken down into three groups: repeatability, stability, and predictability.

3.2.1 Repeatability

A given programming level should always result in the same stored data value, i.e. accurate data programming should be repeatable for a given device. Repeatability includes a given programming pulse storing the same data level regardless of the initial value stored in the device. Given a programming pulse, P_1, which programs a data value of V_1, P_1 should program V_1 into the device, no matter what the data value prior to P_1. Additionally, P_1 should program V_1, regardless how many times the device has been read or programmed by a combination of P_1 and other programming pulses.

3.2.2 Stability

Chalcogenide memory devices should be able to hold the value of the stored data accurately, independent of any environmental changes. While there are many external influences that a device can encounter, a primary factor is time. Ideally, the value of the data stored in the device should not vary with time. Regardless of how long the data value is stored in the device, the exact data value should be retained.

3.2.3 Predictability

The first two analog material properties deal with the ability of a single device to behave as an accurate analog memory. Predictability mandates that an entire array of devices has the same repeatability and stability properties outlined in sections 3.2.1 and

3.2.2. The behavior of one device should be consistent with the behavior of all the other devices created in a fabrication process. The only way designers can produce a memory system that utilizes a specific analog memory is if the designers can accurately predict how every device will perform given a set of programming pulses. Ideally, a model can be developed that describes the devices characteristics accurately enough to allow designers to look at the behavior of a system of devices prior to any manufacturing.

3.3 Characterizing Analog Memory Properties

A characterization approach must be developed to investigate how well the characteristics of chalcogenide memory devices meet the analog memory properties outlined in section 3.2. The characterization approach describes which characterizations should be conducted on the chalcogenide memory devices to determine how the device's performance meet the repeatability, stability and predictability requirements of analog memories.

3.3.1 Programming and Reading Chalcogenide Memory Devices

The programming of chalcogenide memory devices consists of supplying energy to the chalcogenide material to induce a phase-transition discussed in section 2.2.3. A review of the phase-switching behavior is given here with special emphasis on describing the switching in the memory devices.

Published literature has shown that chalcogenide memory can be programmed by applying dc voltage pulses across a load resistor in series with a memory device [3]. The voltage pulse delivered across the load resistor creates a current pulse across the memory

device. The energy supplied by different voltage/current amplitudes for different amounts of time induces a phase change in the material of the memory device. At one extreme, a short, high current pulse will supply the material with a large amount of energy sufficient to vitrify the material. A rapid trailing edge on the pulse quenches the material in its high resistance, amorphous state. At the other end, a lower current pulse, with a longer trailing edge time constant will permit the material to crystallize. The longer pulse with the lower amplitude gives the material enough thermal energy to break the bonds of weakly bonded atoms, but the pulse length allows the atoms to align in the low energy poly-crystalline state. By using voltage pulses with different amplitudes and widths, data values can be written into the chalcogenide memories in the form of resistance values.

Reading the data values from the memory can be done simply by applying a low level read voltage to the device and calculating the resistance value by measuring the voltage drop across the memory device. The applied reading voltage must be below the lowest programming level of the device. If the reading voltage is not below this level, then reading the device will cause the stored data value to change.

For chalcogenide memory devices used in digital applications, only two programming pulses are required: a reset pulse to program the devices to a highly amorphous state and a set pulse to program the devices to a highly crystalline state. The set and reset pulses switch the device between the two extremes of amorphous and poly-crystalline structure. While the switching between highly amorphous and poly-crystalline states is done within a small range of programming voltages, a large number of intermediate resistive values exist between these extremes. By applying voltage pulses

with slight changes in amplitudes, resistance values between the extremes can be programmed into the memory device. Because the memory now can be programmed with a varying degrees of amorphous and crystalline structure, instead of a simple "high" or "low," the memory device can be used for analog data storage.

However, in order to use a memory device as an analog memory, the material must demonstrate the properties necessary for an accurate analog memory: repeatability, stability and predictability.

3.3.2 Repeatability

The first analog memory property that will be investigated is repeatability. Chalcogenide memory devices can be readily programmed between high and low resistance values. However, some preliminary review of the device performance indicates that there are variations in the programmed levels during multiple programming routines [2]. For example, a reset pulse may program a device to a 50kΩ value. The same reset pulse applied later may program the same device to a 72kΩ value. While this 22KΩ difference is not significant for digital applications, the difference can be very significant for analog applications.

Investigating the repeatability of a device requires that identical programming pulses be applied to a device and the resultant resistance values recorded and compared. The pulses should be applied consecutively to ensure the successive pulses of the same programming amplitude does not change the programmed resistance. Additionally, the programming pulses should be applied successively after programming the device to another intermediate value. Applying the programming pulses from different initial

resistance values measures the device's ability to achieve the same programmed resistance value independent of the pre-programmed resistance value.

3.3.3 Stability

Chalcogenide memory devices must demonstrate the ability to retain a stored data value over time in order to be used as an analog memory. Due to the bond breaking and realignment associated with programming chalcogenide memory switches, they have shown excellent time stability. However, the devices have shown a slight drift in resistance levels with time [2]. While the amount of drift in the stored value may be inconsequential for digital memories, it may be substantial for analog applications. The quantity of the potential drift associated with time can be investigated by programming devices to specific levels in between the high and low states and measuring the resultant resistance level at numerous time intervals ranging from a few minutes to several days.

3.3.4 Predictability

Variances in the repeatability and stability between devices can be great despite the fact that all of the chalcogenide memory devices in an array are prepared at the same time. In digital memories that use chalcogenide memory switches, variances in repeatability and stability may not cause a significant problem. For example, if a digital memory device is considered to be in an "off" state (i.e. high resistance) when the programmed resistance value is above 50kΩ, then it does not matter if the identical programming pulse sets the resistance values of two different devices to 55kΩ and 1MΩ. Since both programmed resistance values are higher than 50kΩ, both are considered to be

in an "off" state, even though the actual values of the two resistances differ significantly. In an analog memory device, the difference between a 55kΩ and 1MΩ programmed value for the same programming pulse can be a significant problem. If two devices are programmed to hold the same data value by being programmed with the same programming pulse, but store a different resistance value, then the programmer cannot be sure of the exact value that is stored in each memory device. Since analog data that is read out of a memory location could be different then what was expected, programs using these memory devices could operate on inaccurate data, leading to inaccurate program results. The predictability of the devices can be evaluated by comparing the results of identical repeatability and stability characterizations conducted on different memory devices.

Additionally, the resolution of the analog storage capabilities of the material needs to be compared between different devices. Programming several devices with programming pulses at the highest resolution of the programming pulse generator will help determine the resolution of the memory devices.

3.4 Characterization Approach Summary

The ideal analog memory properties discussed in section 2.3.1 can be divided into two broad categories, those that involve programming the device and those that involve the material properties. The material properties of analog memories can be further sub-divided into these distinct groups: repeatability, stability and predictability.

A characterization approach can be developed by reviewing the limited documented behavior of chalcogenide memory devices along with examining the

material properties of analog memories. The characterization approach describes which experiments are best suited to determine the device's suitability for an analog memory application. From this characterization approach a specific characterization plan was developed, outlining the characterization protocols for the actual device characterizations.

4. Characterization Plan

4.1 Introduction

Characterization protocols are constructed from the characterization approach developed in Chapter Three. This chapter describes each of the characterization protocols used to implement the characterizations outlined in Table 1. The protocols include the purpose and a general description of the characterization, as well as the step-by-step procedure for conducting the characterization.

Table 1. Characterization Matrix

	Repeatability	Stability	Predictability
Programming Pulse Amplitude	x	x	x
Programming Pulse Width	x	x	x
Multiple Read	x		x
Multiple Program	x		x
Programming Pulse Amplitude Step Increase	x		x
Time		x	x
Analog Resolution			x

4.2 Characterization Plan

Before outlining the characterization protocols that are needed to conduct the characterizations developed in the characterization approach, it is first necessary to

describe the exact devices characterized and how the characterizing will be accomplished.

4.2.1 Characterization Devices

The chalcogenide memory devices used in this characterization are prototypes and were designed and supplied by Ovonyx, Inc. [28]. Ovonyx is currently experimenting with two varieties of chalcogenide memory devices: the thin film device and the thick film device. The thin film device has already shown itself useful as a nonvolatile digital memory and is specifically designed to have a very sharp transition between the set and reset states. In the thin film device, a programming voltage increase as small as 0.05V can switch the device between a low resistance and a high resistance value [2]. On the other hand, the thick film device is designed to have a much more gradual transition from the set state to the reset state. In these devices, it takes more than a 1V increase in the programming voltage to switch the device from the lowest resistance to the highest resistance value [2].

Preliminary investigations of thick film devices indicate that the devices may meet the analog material properties of repeatability, stability and predictability discussed in section 3.2. A review of the preliminary data demonstrates that repeated, identical programming pulses will result in similar resistance values in a single device and between multiple devices [2]. Additionally, the devices have excellent data retention over time [2].

The thick film chalcogenide memory devices also have other desirable characteristics which correspond to the externally programming properties described in

section 3.2. The devices have low programming voltages of less than 4V that are approximately the same as the operating voltages of many electronic circuits. The devices are easily programmed with dc voltage pulses and require little additional circuitry for either programming or reading.

Characterizing thick film chalcogenide memory devices should reveal if the devices demonstrate acceptable repeatability and time stability. The predictability of the thick film devices may show changes in the programmed resistance value that would prove to be unacceptable for an accurate analog memory. Since the memory devices supplied are prototype devices, the memory devices may or may not demonstrate predictability. The predictability between devices is largely dependent on a stable, clean fabrication process. Small differences in the fabrication process can lead to differences in device characteristics. When the devices are manufactured in a production quality clean-room facility, the predictability between the devices should improve. Additionally, each of the prototype devices is fabricated with a layer of silicon nitride between the chalcogenide material and the device electrodes. The silicon nitride layer must be punched through by a "first-fire" voltage pulse to allow the device to operate. The first-fire pulse creates a small device area, estimated to be between 2000Å and 2500Å, for the crystalline filament formation [29]. Since each device is formed independently, variations in the operating area between different devices may be significant. The difference in the device area will lead to different behaviors between devices.

The physical structure of the chalcogenide memory devices is proprietary Ovonyx information and therefore cannot currently be published. However, a notional device

structure is given in Figure 12. The device is relatively simple to fabricate with the chalcogenide material being deposited (through sputtering) between the electrodes.

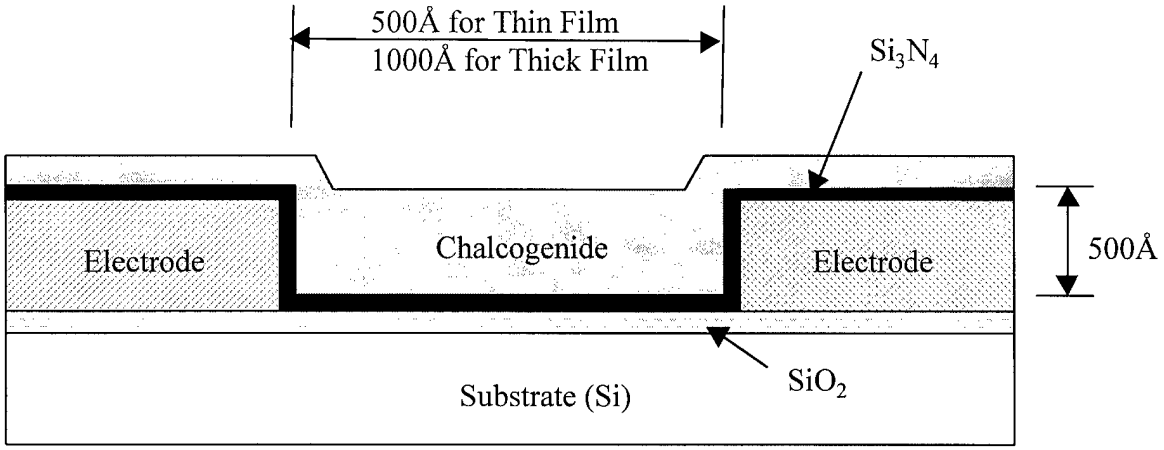


Figure 12. Possible chalcogenide memory device structure

Both the thin film and the thick film prototype memory devices manufactured by Ovonyx come in a square 32x32 two-dimensional array. However, not all 1024 memory devices are addressable. Of the 128 output pads tied to the memory devices, 64 have been connected together to form a common ground. By using so many output pads for a common ground, only 64 devices are available for characterization by using the output pads provided. The characterization device came pre-packaged in a 24-pin integrated circuit chip. Of the 24-pins available on the chip, two are used for ground, leaving 22 devices connected to the input/output pins.

4.2.2 Characterization Circuit

The characterization of chalcogenide memory devices consists of applying dc voltage pulses of varying amplitudes and widths to the device to change its resistivity. A

continuous dc voltage, well below the programming voltage, can then be used to read the programmed resistance of the device. All device characterization utilizes the basic circuit shown in Figure 13.

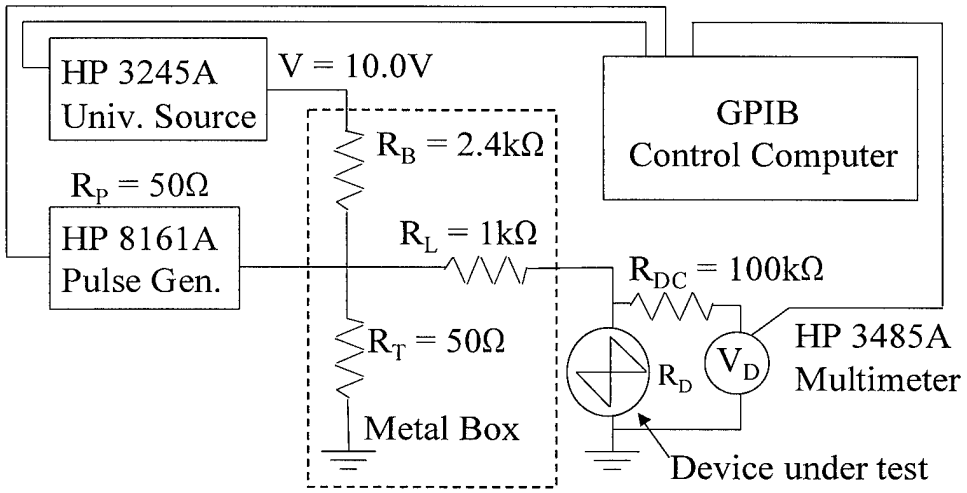


Figure 13. Chalcogenide device characterization circuit

The dc pulse generator is a HP 8131A Programmable Pulse Generator that is capable of providing dc voltage pulses from 0.05V to 5.2V, with a resolution of 0.01V [31]. The dc continuous voltage source is a HP 3245A Universal Source [32] and the voltmeter used to read the voltage across the memory device is a HP 3485A Multimeter [33]. The load resistor, R_L, is used to supply the current pulse needed to induce the phase-shifting in the material. Since device programming is very sensitive to the trailing edge length of the programming pulse, the capacitance of the voltmeter leads is isolated from the rest of the circuit with a 100kΩ decoupling resistor, R_{DC}. R_{DC} allows the trailing edge of the pulse to be as short as possible, set by the pulse generator as no greater than 100ps. The resistor ladder used to characterize the memory devices are

contained in metal box to help shield as much of the circuit as possible from electromagnetic radiation.

Using loop analysis on the equivalent circuit shown in Figure 14, the following equations can be derived:

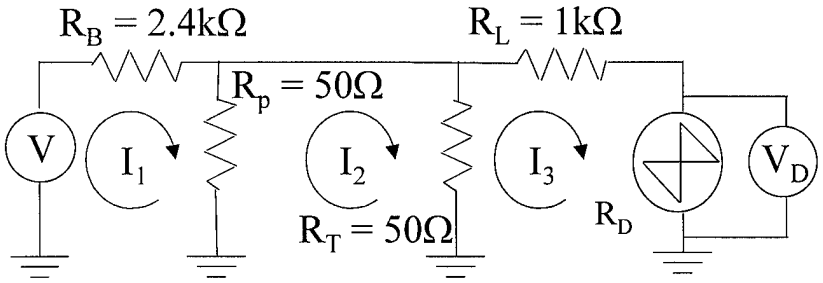


Figure 14. Equivalent characterization circuit

$$V = I_1 R_B + (I_1 - I_2) R_P \tag{2}$$

$$0 = (I_2 - I_1) R_P + (I_2 - I_3) R_T \tag{3}$$

$$0 = (I_3 - I_2) R_T + I_3 R_L + V_D \tag{4}$$

Solving equation (2) for I_1 and substituting into equation (3) yields:

$$I_2 = \frac{V R_P}{R(R_B + R_P)} + \frac{I_3 R_T}{R} \tag{5}$$

where R is:

$$R = \frac{R_P^2}{(R_P + R_B)} + R_P + R_T \tag{6}$$

Substituting (5) into (4) yields:

$$I_3 = \frac{V R_P R_T}{R(R_P + R_B)} - \frac{V_D}{R_T + R_L - R_T^2 / R} \tag{7}$$

Since $I_3 = V_D / R_D$, equation (7) can be solved for R_D:

$$R_D = \frac{(R_T + R_L + R_T^2 / R) V_D}{V R_R R_T / R(R_P + R_B) - V_D} \tag{8}$$

Substituting in the values of the resistors reveals a simple equation that can be used to calculate the resistance of a memory device from the measured voltage across the device:

$$R_D = \frac{1025 \cdot V_D}{0.0101 - V_D} (\Omega) \tag{9}$$

Using the circuit given in Figure 13, programming a thick film chalcogenide memory device consists of applying programming pulse with the HP 8131 while the HP 3245 applies a 10V reading voltage. Reading the resistance of the memory device is accomplished by reading the voltage across the device with the HP 3485, while the output of the HP 8131 is enabled and the HP 3245 is applying a 10V output voltage. The measured device voltage (V_D) is then used in equation (9) to calculate the programmed resistance of the device (R_D). The 10V output from the HP 3245 is reduced at the device to 0.1V by the resistor ladder. The 0.1V value is well below the programming threshold voltage of the device and should not affect the programmed resistance value.

All of the characterizations are controlled by a computer driving control signals through a general purpose interface bus (GPIB). The GPIB control computer interfaces with all of the characterization equipment to sequence and control the programming and reading of the memory devices. The computer runs the LabVIEW© programming software [30] which controls the measurements and calculates device resistances.

4.3 Characterization Protocols

The protocols for the initial device characterization and each of the other characterizations specified in the characterization approach is developed in this section. The initial characterizations determine the programming values (both voltage amplitude

and pulse width) that will be used for the rest of the characterizations performed on the device. After the initial characterizations are complete, the repeatability, stability and predictability characterizations is described. LabVIEW© programs were written for all of the characterization procedures developed in this section and execute the characterizations autonomously without any required intervention.

4.3.1 Initial Programming Pulse Parameter Characterization

Some initial device parameters must be investigated before examining the device's analog memory properties. The initial parameter characterizations reveal the proper, most efficient programming pulses for the devices. Additionally, the parameter characterizations will determine the range over which the devices can be reliably programmed without damage. The two primary parameters investigated are the programming pulse amplitude and the programming pulse width. Results similar to the preliminary data are expected, with programming voltages ranging from 0.5-2.5V and reset pulse widths between 100 and 200ns.

4.3.1.1 Programming Pulse Amplitude

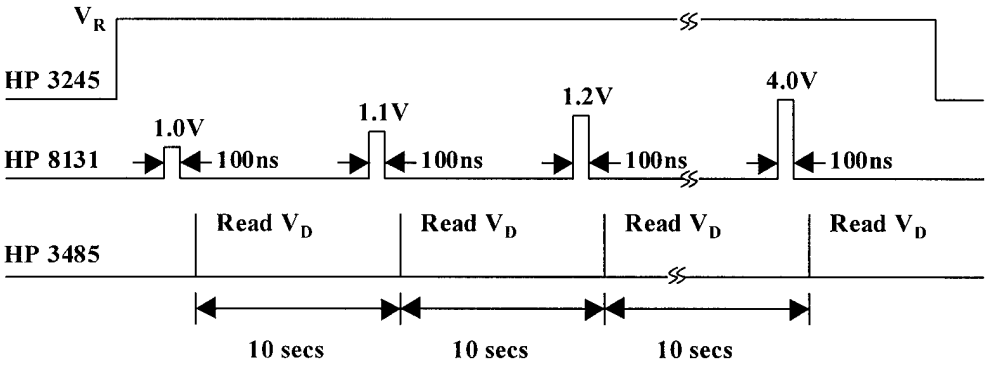
Purpose: The pulse amplitude characterization will determine the range of programming pulse amplitudes needed to program a device from a set state to a reset state.

Description: The pulse amplitude characterization begins with a device in a high resistance state. Programming pulses of increasing amplitudes will then be applied to the device, starting at 0.05V and ending at 4.0V. For all programming pulses, the pulse

width is at 100ns. The range of programming levels for the device is determined by examining the reaction of the device to the different programming levels.

Procedure:

1. Apply the read voltage from the HP 3245
2. Apply the programming pulse from the HP 8131 with the set pulse amplitude
3. Measure the voltage across the device and calculate the device resistance



4.3.1.2 Programming Pulse Width

Purpose: The pulse width characterization results will determine the proper pulse widths for programming a memory device.

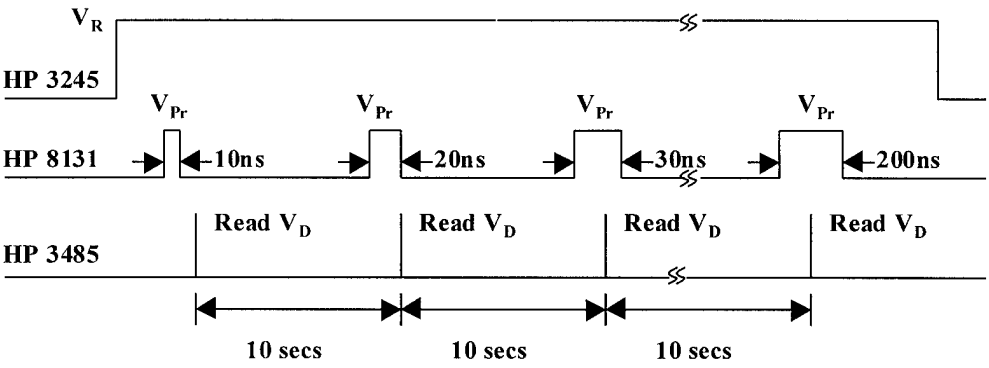
Description: The pulse width characterization consists of two sub-characterizations, one that does not set the device to a low resistance level between programming and another that does. The characterization without the set between programming begins with a device in a high resistance state. The device is then programmed with reset pulses of varying widths, from 10ns to 200ns. For all of the reset programming, the amplitude is the programming amplitude that results in the highest resistance value as determined from the pulse amplitude characterization. The second sub-characterization repeats the first sub-characterization, but sets the devices to a low

resistance state between each reset programming. The set pulse is a 100ns pulse, with the amplitude being the programming voltage leading to the lowest resistance value as determined from the pulse amplitude characterization. The programming width for reset pulses can be determined by examining the results of both of the sub-characterizations. The width that results in the highest resistance value is the proper width to use for the result pulse. Both characterizations are needed to ensure that the initial resistance value of the device, either a high or low resistance, does not affect the reset amplitude.

Procedure:

Programming Pulse Width without Set:

1. Apply the read voltage from the HP 3245
2. Apply the programming pulse from the HP 8131 with the reset pulse width
3. Measure the voltage across the device and calculate the device resistance

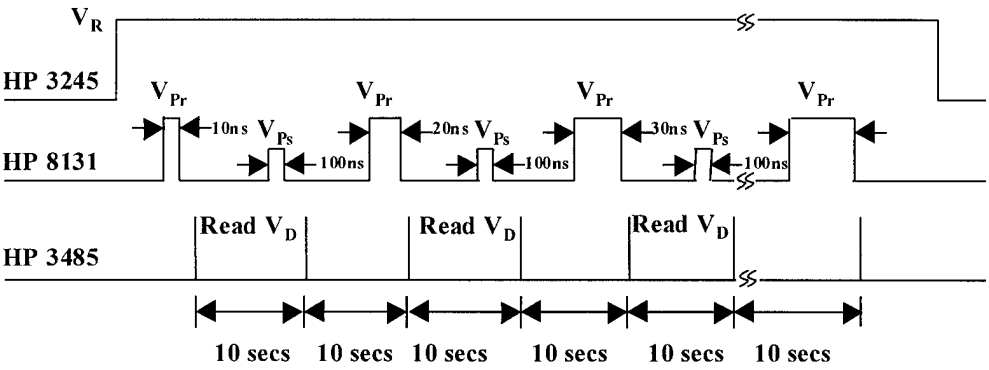


V_{Pr} - the reset amplitude determined from the pulse amplitude characterization

Programming Pulse Width with Set:

1. Apply the read voltage from the HP 3245
2. Apply the programming pulse from the HP 8131 with the reset pulse width

3. Measure the voltage across the device and calculate the device resistance
4. Apply the set programming pulse
5. Measure the voltage across the device and calculate the device resistance



V_{Ps} - the set amplitude determined from the pulse amplitude characterization

4.3.2 Repeatability Characterization

A device must be programmed with the same programming pulse multiple times to measure the repeatability of the memory device. The multiple programming must include programming from different pre-programming levels to ensure that going from any initial resistance level to another is independent of this initial level. After the programming is complete, the results can be compared and conclusions regarding the repeatability are made.

Three characterizations are used to investigate the repeatability of chalcogenide devices. The first characterization, the multiple read characterization, involves continuously reading the memory device without applying any programming pulses, while the second characterization, the multiple programming characterization, involves repeatedly programming the device with the same programming pulse. The third characterization, the programming pulse amplitude step increase characterization (or step

increase characterization), increases the programming voltage of the device in a stepped fashion, from a low voltage to a high voltage. The ramping of the programming voltage is done is small steps to have a good resolution on the behavior of the device.

The chalcogenide memory devices should demonstrate good repeatability, with most programmed resistance values within 5% of the mean resistance value. This value corresponds to approximately a 4-bit resolution for a 10kΩ-1MΩ resistance range. Additionally, since the reading voltage applied to the device will be well below the initial programming levels, the multiple read characterization should not affect the resistance level of the device.

4.3.2.1 Multiple Read

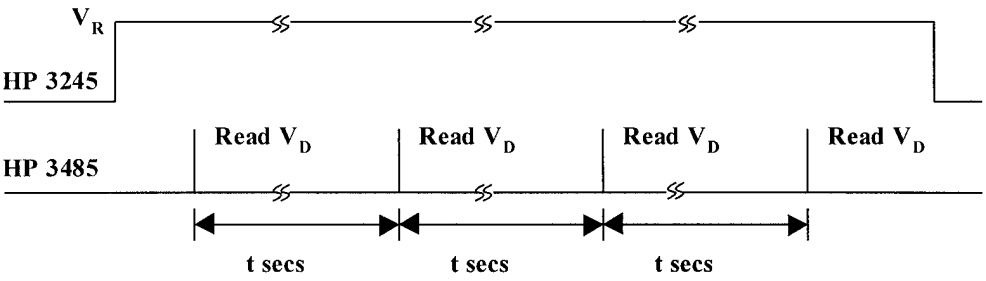
Purpose: The multiple read characterization examines the affect that applying multiple read voltages has on the stored data value in a memory device.

Description: The multiple read characterization consists of two sub-characterizations. The first sub-characterization, the continuous read characterization, continually applies the read voltage to a device set at any resistance value. The resistance of the device is measured at certain time intervals to examine any change that is occurring. The second sub-characterization, the pulsed read characterization, applies a reading voltage of a certain length to the device and then waits a specified amount of time before again applying the read voltage. The affect of an applied reading voltage versus an idle device is observed by comparing the two sub-characterizations. Since the reading voltage is well below the threshold voltage of the device, no change in the set resistance value of the device should be observed.

Procedure:

Continuous Read:

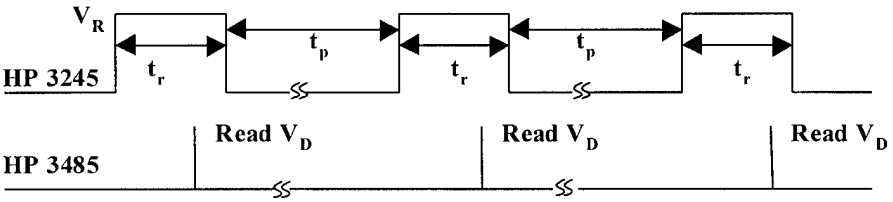
1. Apply the read voltage from the HP 3245
2. Measure the voltage across the device and calculate the device resistance



t secs - measure the voltage across the device every t secs

Pulsed Read:

1. Apply the read voltage from the HP 3245
2. Measure the voltage across the device and calculate the device resistance
3. Remove the read voltage



t_r - time to apply the read voltage

t_p - time between read voltage applications

4.3.2.2 Multiple Program

Purpose: The multiple program characterization examine the affect applying multiple programming pulses has on the programmed resistance level. Each

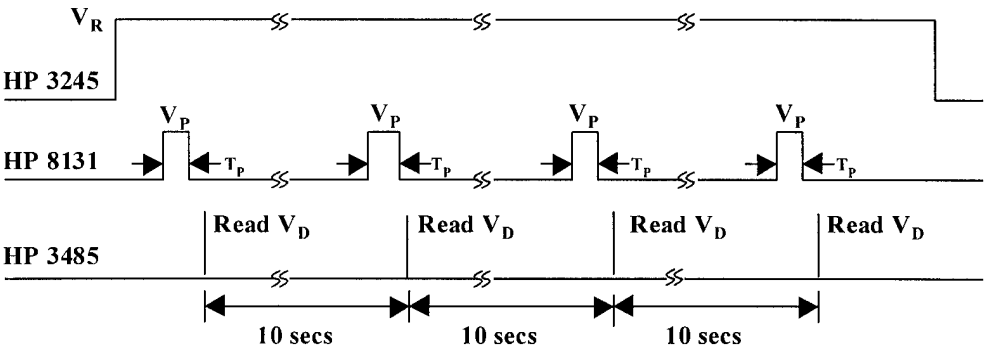
programming pulse has the same amplitude and width, and therefore should program the device to the same resistance value.

Description: The multiple program characterization consists of two sub-characterizations, with each sub-characterization beginning with a device set to any resistance value. For the first sub-characterization, a programming pulse is repeatedly applied to the device without resetting the device to a high resistance level between programming. For the second sub-characterization, the first sub-characterization is repeated, but the device is reset to a high resistance value between each programming step cycle. Since in both sub-characterizations the programming pulse amplitude and width are not changed, the device should be repeatably programmed to the same resistance value. The affect of the pre-programmed resistance value, either the set resistance or reset resistance value, can be examined by comparing the two sub-characterizations.

Procedure:

Multiple Programming without Reset:

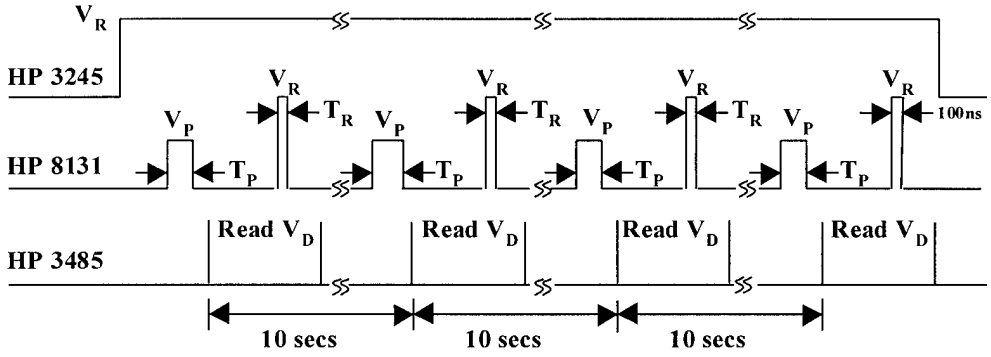
1. Apply the read voltage from the HP 3245
2. Apply the set programming pulse from the HP 8131
3. Measure the voltage across the device and calculate the resistance



V_P - the set amplitude
T_P - the set pulse width

Multiple Programming with Reset:

1. Apply the read voltage from the HP 3245
2. Apply the set programming pulse from the HP 8131
3. Measure the voltage across the device and calculate the resistance
4. Apply the reset programming pulse from the HP 8131
5. Measure the voltage across the device and calculate the resistance



V_P - the set amplitude
T_P - the set pulse width
V_R - the reset amplitude
T_R - the reset pulse width

4.3.2.3 Programming Pulse Amplitude Step Increase

Purpose: The programming pulse amplitude step increase characterization (or step increase characterization) measures the ability of the device to achieve the same

resistance level given identical programming pulses where the amplitude of the programming pulses are applied in a increasing step fashion.

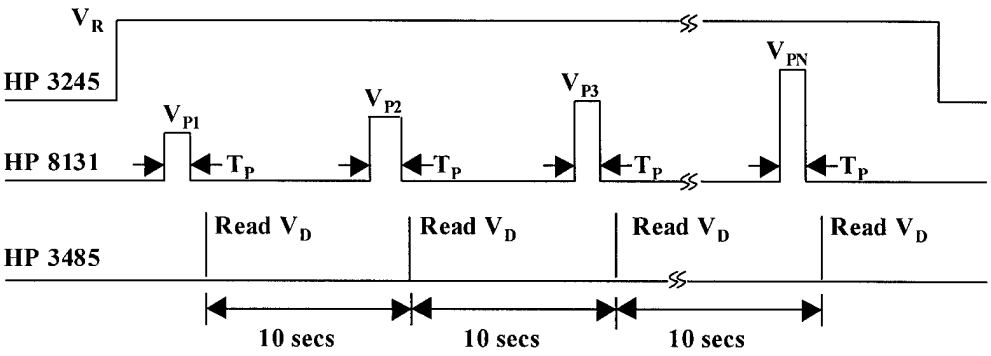
Description: The step increase characterization consists of two sub-characterizations, each beginning with a device in a high resistance state. The first sub-characterization applies programming pulses to the device with the amplitude of the pulse increasing in steps, but does not reset the device to a high resistance state between programming. The programming range should begin with a programming voltage lower than the threshold voltage and end when the programmed resistance values reach a saturated level. For a memory device, the resistance values set by the same programming pulses for repeated characterizations should be the same.

The second sub-characterization repeats the step increase without reset characterization, but adds the additional step of resetting the device to a high resistance value between each applied programming pulse. The voltage amplitude and width of the reset pulse will be determined from the initial parameter characterization. As with the step increase without reset characterization, the resistance values of the given programming pulses for repeated characterizations should be the same.

Procedure:

Programming Pulse Amplitude Step Increase without Reset:

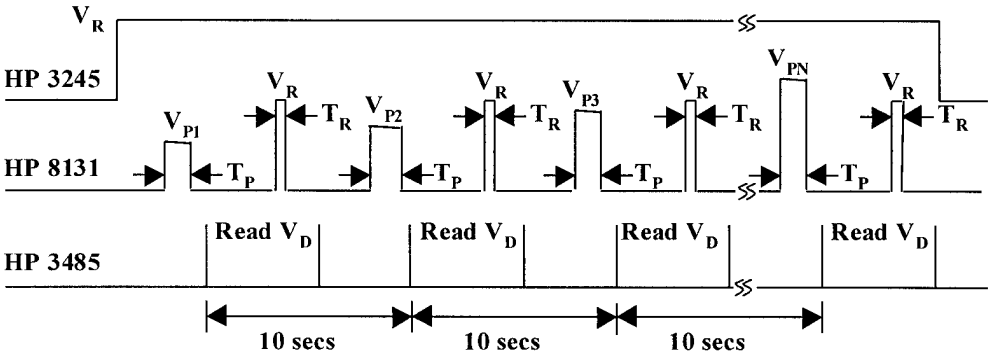
1. Apply the read voltage from the HP 3245
2. Apply the set programming voltage pulse from the HP 8131
3. Measure the voltage across the device and calculate the resistance



$V_{P\#}$ - set amplitude, increased step wise as determined from the initial parameter characterizations
T_P - the set pulse width

Programming Pulse Amplitude Step Increase with Reset:

1. Apply the read voltage from the HP 3245
2. Apply the set programming pulse from the HP 8131
3. Measure the voltage across the device and calculate the resistance
4. Apply the reset programming pulse from the HP 8131
5. Measure the voltage across the device and calculate the resistance



$V_{P\#}$ - set amplitude, increased step wise as determined from the initial parameter characterizations
T_P - the set pulse width
V_R - the reset amplitude
T_R - the reset pulse width

4.3.3 Stability Characterization

A stability characterization can be conducted to examine the temporal stability of the chalcogenide memory devices. This characterization simply looks at the resistance value of a device over time to see if any changes in the resistance value occurs. Since chalcogenide memory devices have shown excellent time stability in preliminary investigations [2], no significant change in resistance levels is expected.

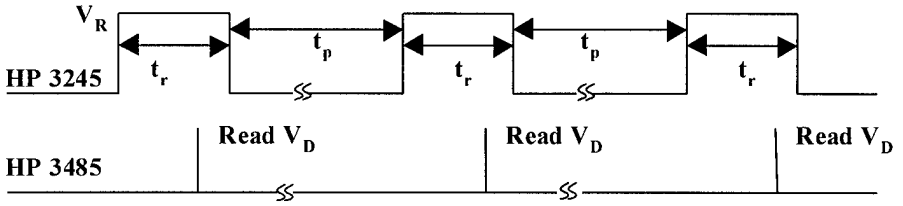
4.3.3.1 Time Stability

Purpose: The time characterization is used to investigate the ability of the memory device to hold a programmed resistance value.

Description: The time characterization is a simple characterization where a memory device is initially set to a specific resistance value. The resistance of the device is then measured at different time intervals. To provide a more complete characterization, memory devices set to resistance levels between the low and high values should be used. Repeating the characterization with different resistance values will help determine if higher or lower resistance values are any more susceptible to changes over time. Since chalcogenide memory devices have shown excellent time stability, neither high or low resistance values show a change over time.

Procedure:

1. Apply the read voltage from the HP 3245
2. Measure the voltage across the device and calculate the resistance
3. Remove the read voltage from the HP 3245
4. Wait for a specified amount of time



t_r - time to apply the read voltage

t_p - time between read voltage applications

4.3.4 Predictability Characterization

The results of the repeatability and stability characterizations are used to examine the predictability of chalcogenide memory devices by comparing the results of the characterization described in sections 4.3.2 and 4.3.3 for different devices. Since the fabrication of the prototype chalcogenide devices is not as tightly controlled as production quality fabrication process, the repeatability and stability characterization resistance values may not correspond very well. Therefore, the predictability of the memory devices may not be good. Significant differences are expected between identical characterizations of different devices.

In addition to comparing the results of the repeatability and stability characterizations the analog resolution for each device is examined. This characterization will determine if the devices have a sufficient resolution to accurately store analog values and if each device has the same resolution.

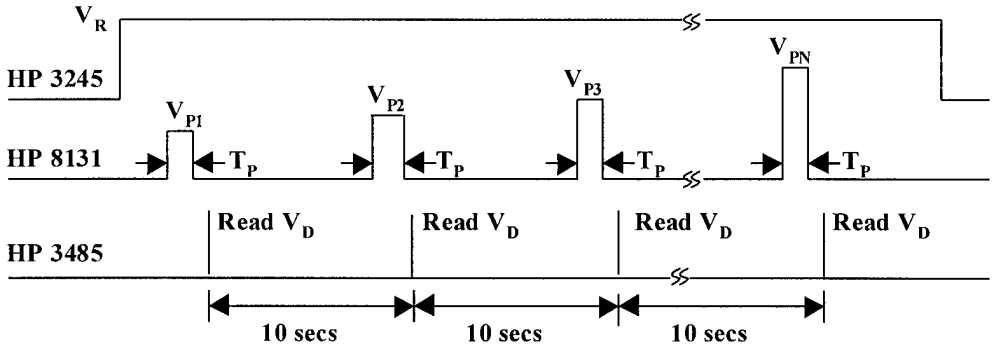
4.3.4.1 Analog Resolution

Purpose: The analog resolution characterization will determine how many discrete resistance levels can be programmed into a memory device.

Description: The analog resolution characterization will look specifically at the range of programming voltages that result in the best analog memory behavior, at the highest resolution of the pulse generator. For this characterization, the step increase without reset characterization will be repeated. However, the voltage increment is reduced to the smallest allowed by the pulse generator (0.01V). Since the chalcogenide memory devices being characterized are a thick film devices, an exponential increase from the low resistance value to a high resistance reset value is expected.

Procedure:

1. Apply the read voltage from the HP 3245
2. Apply the set programming pulse from the HP 8131
3. Measure the voltage across the device and calculate the resistance



$V_{P\#}$ - set amplitude, increased step wise as determined from the initial parameter characterizations at minimum resolution of the pulse generator
T_P - the set pulse width

4.4 Characterization Plan Summary

This chapter introduces the characterization plan that is followed to characterize the chalcogenide memory devices. In additional to describing the protocols used in the

characterizations, the chapter also provides a description of the devices and the characterization circuit.

Currently, Ovonyx, Inc. fabricates two prototypes of chalcogenide memory devices. The first type is a thin film device with a small programming range between the high and low resistance values and is primarily used for digital applications. The second type is a thick film device that has a larger range between the high and low resistance values and may be more applicable to analog circuits. The memory device are characterized using the characterization circuit described in Figure 13. All characterizations are controlled by a control computer running LabVIEW© programming software to program and automate the characterizations.

Eleven characterizations were developed to examine the repeatability, stability and predictability of the memory devices. Ten of these eleven characterizations examine the response of different memory devices to investigate the possibility of different programming levels. The other characterization measures the ability of a device to retain a set resistance level over time.

The characterization protocols described in this chapter do not provide an exhaustive list of characterization possibilities. However, the protocols provide an excellent foundation to make observations regarding the ability of chalcogenide memory devices to perform as an accurate analog memory. The results of the characterizations and analysis of these results is provided in the next chapter.

5. *Characterization Results and Analysis*

5.1 Introduction

The outcome of the characterizations described in section 4.3 yielded some surprising results. Initial device measurements were accomplished on thin film chalcogenide memory devices because the thin film devices were available earlier than the thick film devices. The thin film devices were used to construct and validate the characterization equipment and circuit, and to conduct the multiple read characterizations. The initial characterizations of the thin film devices revealed several challenges that were overcome before automated characterizations could be conducted. The rest of the repeatability, stability and predictability characterizations were conducted after the thick film devices were received.

The initial parameter characterization was the first characterization conducted on the thick film chalcogenide devices, followed by the programming pulse amplitude step increase, multiple programming and analog resolution characterizations. The time characterization was the last characterization conducted. Sixteen thick film and three thin film devices were used to conduct the characterizations. Not all the characterizations described in section 4.3 were conducted on all nineteen chalcogenide devices, rather the characterizations were spread among the devices tested. Typical characterization results and analysis of the results for the repeatability, stability and predictability characterizations conducted in this research are provided in section 5.2.

5.2 Characterization Results

The results of the initial parameter characterizations conducted on the thick film chalcogenide memory devices were used to verify the operation of the devices and to determine the correct parameters for the programming pulses. Thick film devices were then used to conduct the programming pulse amplitude step increase and multiple programming characterizations, by using the characterization procedures specified in section 4.3 and the results of the initial parameter characterizations. After the repeatability characterization was complete, the time and analog resolution characterizations were conducted to characterize the devices for stability and predictability.

Multiple read characterizations were conducted on the thin film chalcogenide memory devices because the thick film devices were not initially available. Since the multiple read characterization does not actively program the device, the structures of the devices are similar and the read voltages of the devices are the same, it is valid to extrapolate the results of the thin film multiple read characterization to the thick film devices.

5.2.1 Initial Programming Pulse Parameter Characterization Results

Initial device performance parameters were investigated before examining the device's analog memory properties. The initial parameter characterizations revealed the proper, most efficient programming pulses for the devices. Additionally, the parameter characterizations also determined the range over which the devices are reliably programmed without over-stressing the material. The two primary parameters

investigated were the programming voltage pulse amplitude and the programming voltage pulse width.

5.2.1.1 Programming Pulse Amplitude

The results of the pulse amplitude characterization described in section 4.3.1.1 are shown in Figure 15. Figure 15 displays the average of ten characterization runs conducted on two different thick film chalcogenide memory devices. All of the programming for this characterization was done at a fixed programming pulse width of 100ns.

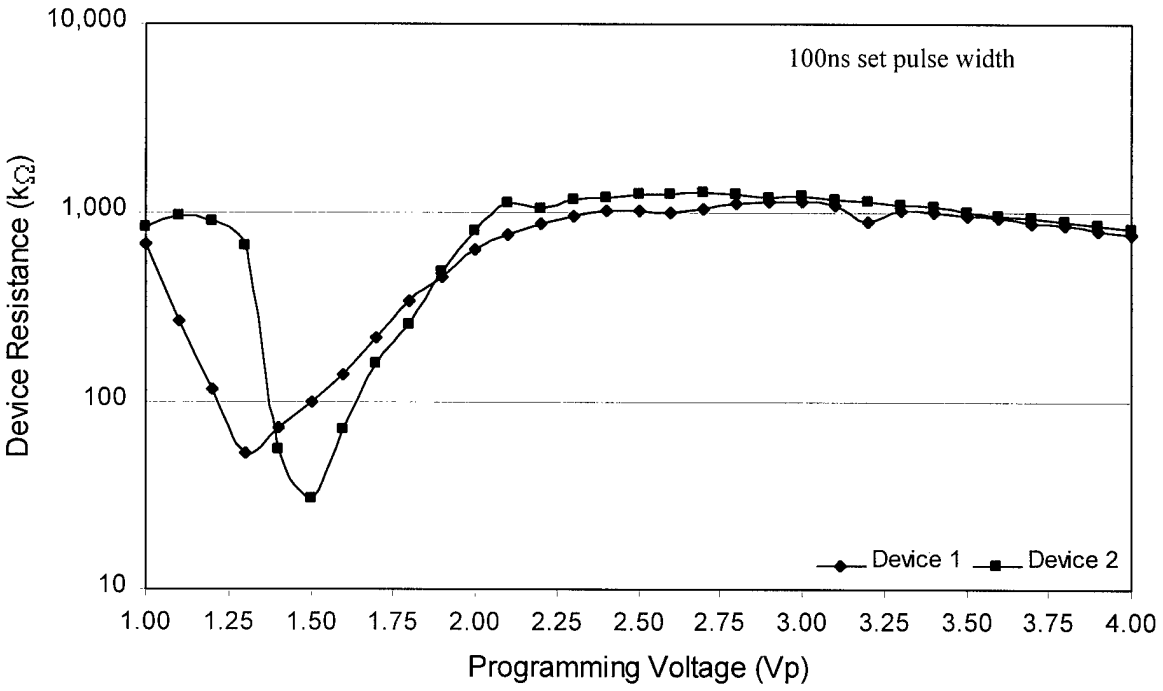


Figure 15. Representative programming pulse amplitude results

The results show the programming ranges of the devices are between the threshold voltage, approximately 1.0-1.3V, and 2.5V. At the threshold voltage, the

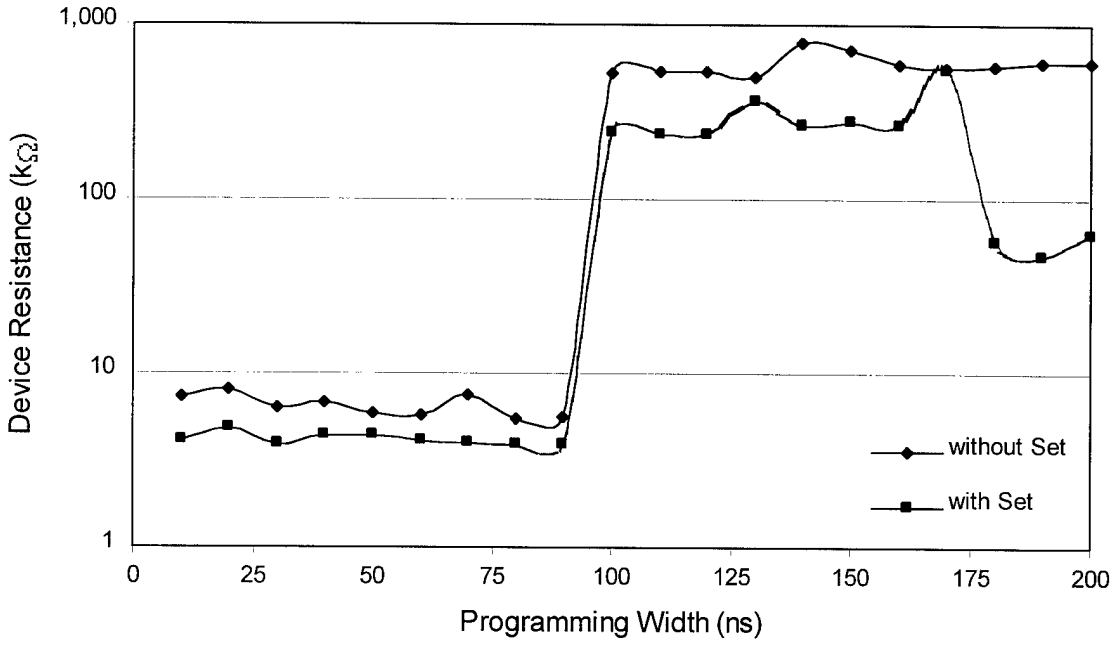
programming pulse supplies the chalcogenide material enough thermal energy to break the bonds of the amorphous structure and allows the bonds enough time to realign into a poly-crystalline arrangement. At programming amplitudes below V_{th}, the thermal energy imparted to the material is not enough to break any of the bonds in the amorphous structure, so no change in the organization of the material is accomplished. Since the bonds for programming voltages below V_{th} are unchanged, the resistance of the device remain unchanged.

At programming amplitudes above the threshold voltage, the thermal energy supplied through the programming pulse begin breaking the bonds of the poly-crystalline structure and returning sections of the material to an amorphous state. The steep trailing edge on the programming pulse rapidly reduces the thermal energy and "quenches" or freezes the material at these sites in the amorphous state. As the programming voltage of the pulse is increased more of the material is returned to an amorphous structure, and the resistance of the device increases. At 2.5V, the material is returned to an amorphous state since no further increase in the device's resistance value is seen. Therefore, at voltages above 2.5V, more thermal energy is added to the material, but no further crystalline bond breaking occurs and set programming voltages above 2.5V are not needed. However, to help ensure that the maximum amount of poly-crystalline structure is removed when the device is reset, a reset voltage amplitude of 2.6V is used. The programming pulse width characterization determines the appropriate reset pulse width to obtain the highest amount of amorphous structure in the material, corresponding to the highest device resistance level.

5.2.1.2 Programming Pulse Width

The result of the pulse width characterization described in section 4.3.1.2 are shown in Figure 16. Both characterization runs indicate that the minimum programming width for the highest device resistance, known as the reset pulse width, is 100ns. At pulse widths below 100ns, the thermal energy imparted by the programming pulse is not sufficient break any bonds in the poly-crystalline material and subsequently quench the material into an amorphous state. Pulse widths longer than 100ns can be used but longer pulses do not substantially increase the resistance values of the device. A reduction in the programmed resistance value is seen at the higher pulse widths for the characterization with the set. This reduction is likely caused by too much thermal energy stored in the surrounding material, making the rapid quenching of the material into an amorphous state impossible.

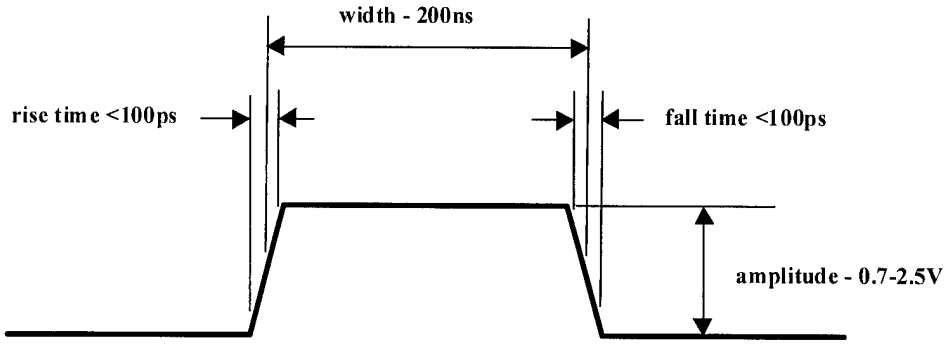
The preliminary data on chalcogenide devices demonstrated that the pulse width to program the device (set pulse width) was obtained by doubling the pulse width needed to reset the device into a high resistance state [2]. Therefore, the lowest possible high resistance pulse width should be used to give the shortest necessary set pulse width. Doubling the 100ns reset pulse width leads to using a 200ns pulse width for device programming. The set programming pulse is longer than the reset pulse to allow the thermal energy more time to break the bonds of the material and then allow the bonds to align in a crystalline structure.



5.2.1.3 Summary of Initial Parameter Characterization Results

The results of the pulse amplitude and pulse width characterizations revealed that the voltage range for programming the thick film chalcogenide memory devices is between the threshold voltage and 2.5V, with a set pulse length of 200ns. Since the threshold voltage for chalcogenide devices vary from device to device, the characterization programming voltage range will begin at 0.7V to ensure the entire programming range, from V_{th} to 2.5V, is captured. Additionally, the reset pulse has a width of 100ns with an amplitude of 2.6V. The parameters determined by this characterization were the programming pulse parameters used for the rest of the chalcogenide device characterization. A schematic of these pulses is provided in Figure 17.

Set Pulse-



Reset Pulse-

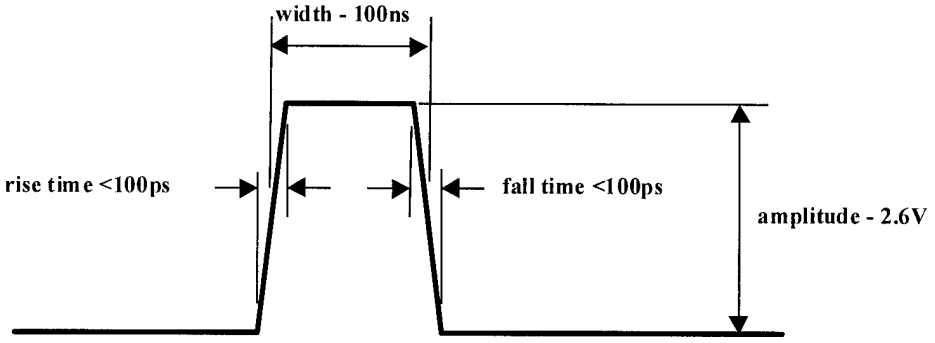


Figure 17. Representation of the programming pulses

5.2.2 Repeatability Characterization Results

Completing development of the programming pulse parameters allowed the characterizations of the analog material properties to begin. The first analog memory property characterized was repeatability. The set of characterizations that determined the repeatability of the chalcogenide memory devices is given in section 4.3.2 and consists of the multiple read, multiple program, and the programming pulse amplitude step increase characterizations.

5.2.2.1 Multiple Read

The multiple read characterization was completed using the thin film chalcogenide memory devices and investigates the affects that reading the device resistance has on the programmed resistance value. Using the results of the thin film characterizations for the analog memory property investigation is acceptable because the characterization does not involve programming the devices. Rather, the devices are subjected to a simple read cycle to determine if the reading pulse energy affects the programmed resistance value. Since the 0.1V read voltage used for both the thin film and thick film chalcogenide devices is well below the threshold voltage of both devices and reading a device should not account for any change in the set resistance value. Additionally, since both types of chalcogenide devices employ the same material in a similar configuration, the results of the thin film characterization are valid for the thick film devices.

A sample result of the first multiple read characterization, which supplies a continuous read voltage for a set length of time, is given in Figure 18. As the results in Figure 18 show, although the reading voltage is well below the threshold voltage, continually applying the reading voltage to the device changed the resistance value stored in the memory device. The characterization in Figure 18 shows the resistance value of the device remaining fixed until there was a rapid drop in the resistance value that reduced the resistance by an order-of-magnitude. After the resistance value drops, the resistance of the device increases to an asymptotic value below the original resistance value of the device.

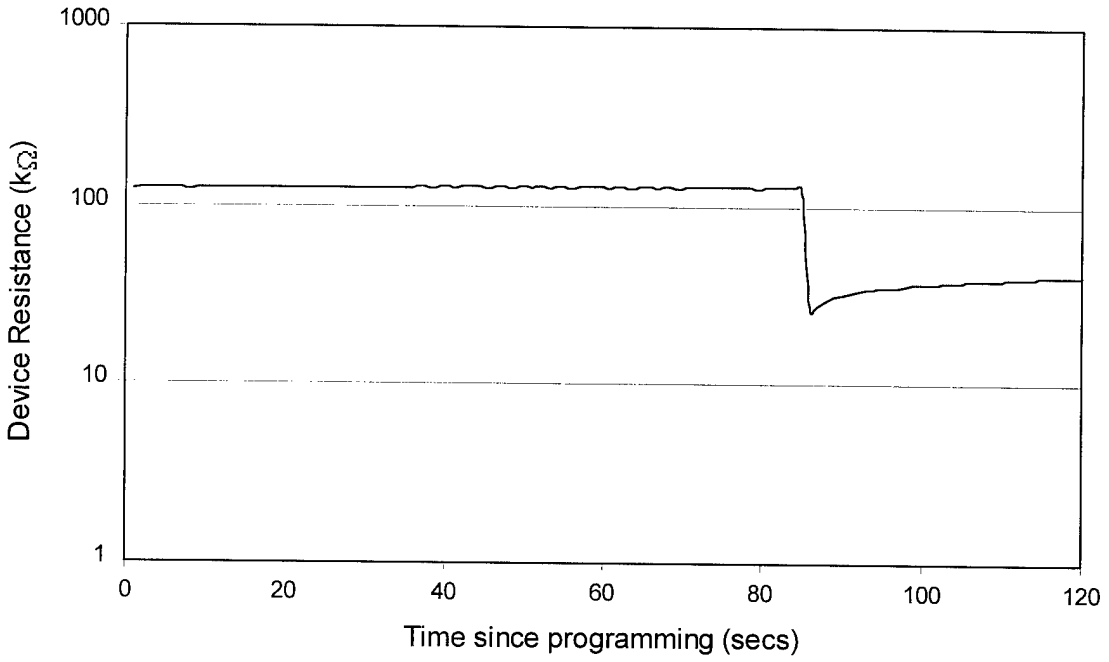


Figure 18. Sample device resistance reduction in the continuous read

Three of the eleven continuous read characterization runs on two different devices demonstrated this behavior, while the other eight characterization runs did not exhibit any change in the measured device resistance. The standard deviation of the eight runs that did not demonstrate the behavior remained within 5% of the average measured device resistance value. The standard deviation used measures how widely values are dispersed from the mean given that the values used are a representative sample of the population. The standard deviation equation is given by:

$$\text{Standard Deviation} = \sqrt{\frac{\sum x^2 - \left(\sum x\right)^2 / n}{n-1}} \tag{10}$$

The pulsed read characterization was conducted by applying a reading voltage pulse of varying widths, with different intervals between reading pulses. The results of pulsed read characterization, shown in Figure 19, are implemented using a three second long read pulse with a five minute period between read pulses. As with the continuous read characterization, the resistance value read in the pulsed read undergoes a rapid reduction at certain points, reducing the resistance value by approximately 50%. After the resistance value of the device shifted, the resistance value slowly increased to a point slightly lower than the previous value.

Two of the six characterization runs demonstrated this type of behavior. The standard deviation of the four runs that did not demonstrate the rapid drop in the device resistance remained within 5% of the average measured resistance value.

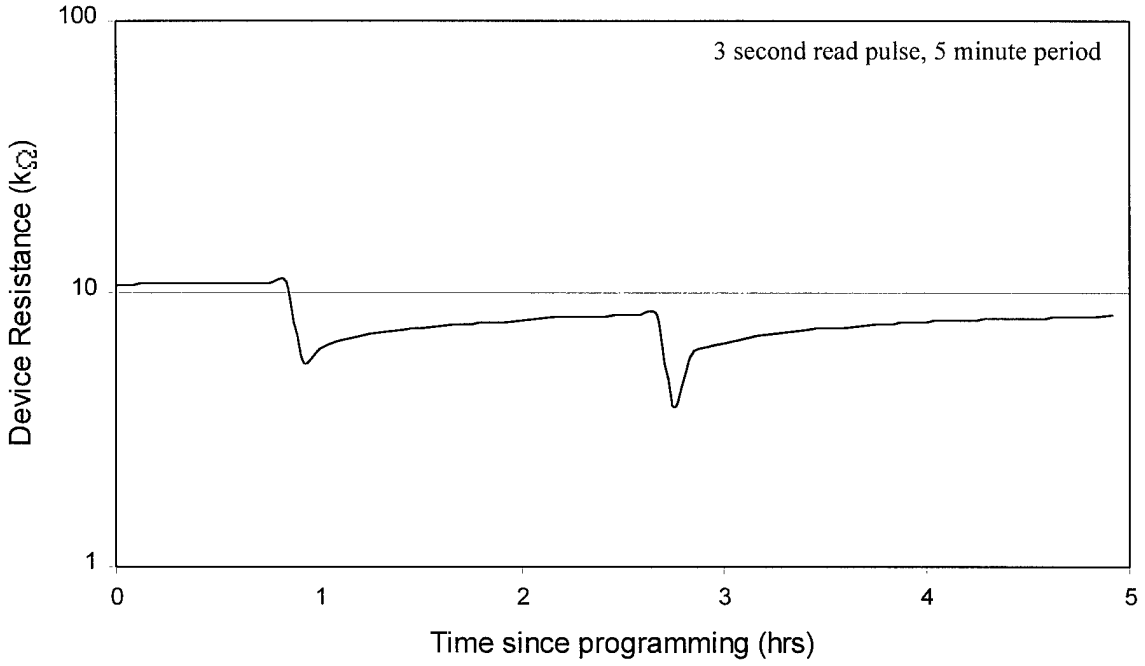


Figure 19. Sample device resistance reduction observed during the delayed read

The drop in the resistance value seen in both the continuous and pulsed read indicate that the low level reading voltage is affecting the chalcogenide material. While the limited set of characterizations cannot conclusively prove what is happening within the material, a likely cause is thermal energy from the applied 0.1V read voltage is inducing a recrystallization. As the read voltage is applied, thermal energy within the material causes and a switching event to occur. During this event, a complete poly-crystalline filament is not formed between the electrodes. Rather, pockets of poly-crystallinity, or micro-crystallites, are formed in the material leading to areas of higher conduction in the material. These sites are not stable and energy during subsequent reads is enough to break down the crystallites and return the sites to a higher resistance level.

The micro-crystallite formation occurs whenever the read voltage is applied. However, a rapid reduction in the resistance of the device is only seen when enough crystallites are formed to provide an additional conduction path through the material. As the data shows, the formation of a secondary conduction path does not always occur and when it does, can occur at seemingly unpredictable times.

5.2.2.2 Multiple Programming

The multiple programming characterization utilized the thick film chalcogenide memory devices and examines the results of programming the device multiple times with the same programming pulse. The results of both the characterizations described in section 4.3.2.2 are presented in Figure 20 and Figure 21. The figures show the maximum, minimum, and mean resistance value of the device for each programming level above the threshold voltage, as well as the standard deviation calculated by equation

(10). The standard deviation is given by the percent of the mean resistance value so it can be compared for different resistance values.

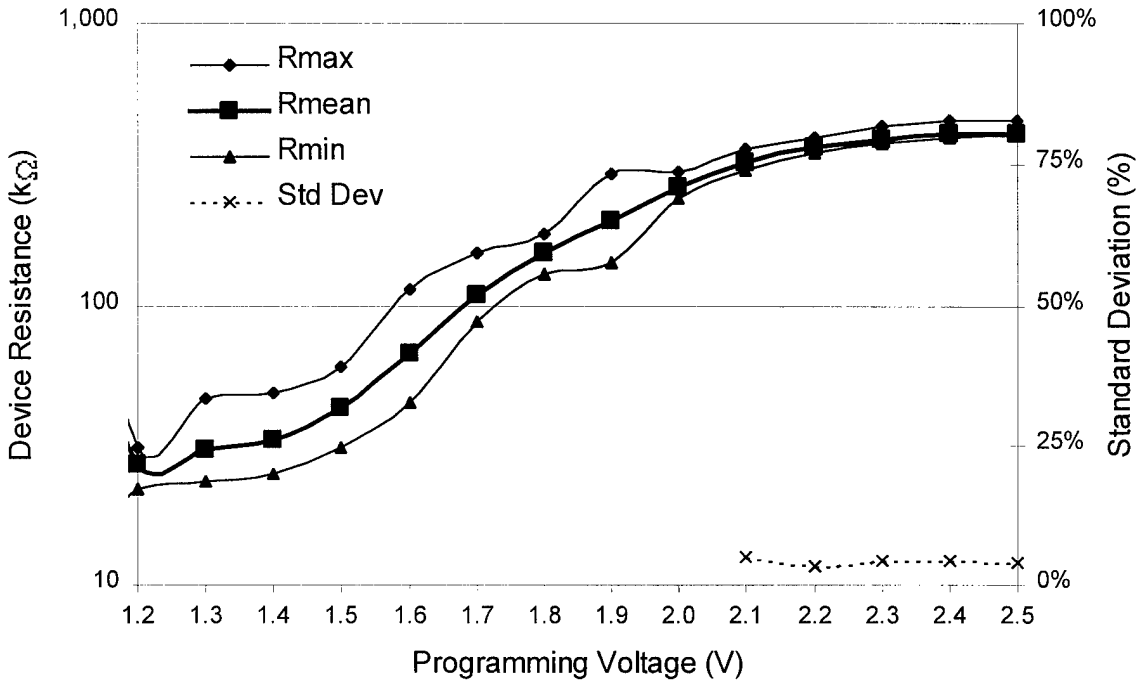


Figure 20. Multiple program without reset results for a single device

The results in Figure 20 and Figure 21 show a single device with programming repeated ten times for each programming voltage level. The same characterizations repeated on another device yield similar results. The standard deviations for the multiple programming with the reset were greater than the multiple programming without the reset. Looking specifically at the programming voltages above the threshold voltage, approximately 1.2V, the average standard deviation for the characterization without the reset was 25%, while the characterization with the reset was 50%. The difference between the characterizations is most easily seen by looking at the resistance values set

by the 2.1-2.5V programming voltages. During this programming range, the characterization without the reset varied by just a few percent, while the characterization with the reset varied up to 45%.

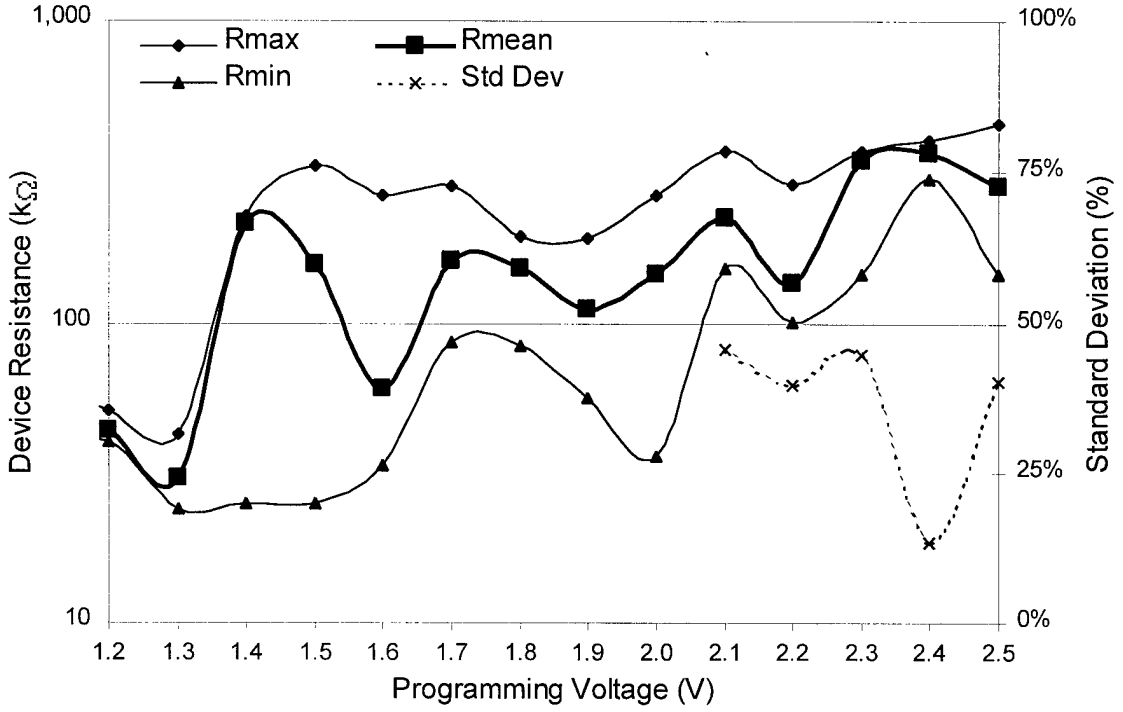


Figure 21. Multiple program with reset results for a single device

In the characterization without the reset, the device is repeatably programmed with identical programming pulses. The initial programming pulse sets the resistance of the material to a certain value. The resistance value depends on the amount of crystallinity left in the material after the thermal energy is supplied by the programming pulse. Each successive identical programming pulse should impart the same amount of thermal energy to the material and therefore the successive pulses should not significantly change the amount of crystallinity in the material. The energy supplied by successive

pulses is not enough to induce significantly more bond breaking and realignment than the initial programming pulse. Since the successive pulses do not substantially change the level of crystallinity, the resistance value of the device will remain unchanged. However, the pulse does allow some changes in the bonding structure along the boundary between the crystalline filament and the amorphous bulk material. The slight variance in the bonding at the boundary, whether more crystalline or more amorphous, will slightly alter the resistance value.

The characterization with the reset showed larger variations in the set resistance values for identical programming pulses. This is expected because between each programming pulse, the device is reset to a highly amorphous state corresponding to a high resistance value. Therefore, each programming pulse in the characterization with the reset has to set the material to a lower resistance value, where the pulses in the characterization without the reset only had to maintain the set resistance value. For the characterization with the reset, each programming pulse will break the bonds of the amorphous material and will realign the bonds into a more crystalline structure along the filament between the electrodes. The amount of poly-crystallinity in the material is dependent on the amount of thermal energy supplied by the programming pulse. A pulse amplitude at the threshold voltage of the material will give the material enough energy to break the bonds and allow the atoms to move into a highly poly-crystalline alignment. At a pulse amplitude voltage higher than the threshold voltage, the energy will break the bonds of the material, but will also supply the atoms of the material with energy for a certain length of time. The energy imparted to the atoms excites the atoms in to a "meta-stable" state and prevents the atoms from aligning into a highly poly-crystalline structure.

The higher the energy supplied to the atoms, the fewer atoms that will be able to align in a poly-crystalline structure and the higher the resistance value of the device. Since the bond breaking and alignment must take place for every programming pulse in the characterization with the reset, the amount of crystallinity programmed into a device varied. The variation in crystallinity was due to the slightly different crystalline filament path formed for each programming pulse in the characterization with the reset. Since each programming pulse for the characterization with the reset formed a new poly-crystalline filament path with differing amounts of crystallinity, each pulse showed different resistance values.

5.2.2.3 Programming Pulse Amplitude Step Increase

Results of the step increase without reset characterization described in section 4.3.2.3 are shown in Figure 22. These results show the average resistance values programmed above the threshold voltage for ten repetitions of the step increase without reset characterization on a single device. The results shown in Figure 22 are typical for the thick film chalcogenide devices and were seen in all three of the devices tested. Figure 22 shows a narrow gap between the minimum and maximum values for the ten runs examined. This narrow gap corresponds to a fairly tight range of resistance values for the given programming pulses. The tight range of values indicates that the material responds well to the programming pulse increase over the programming range.

For two of the devices, the device resistance set by each of the programming pulses was progressively lower for each repetition of the characterization. Figure 23

shows the reduction in the device resistance over the repetition of the step increase without reset characterization.

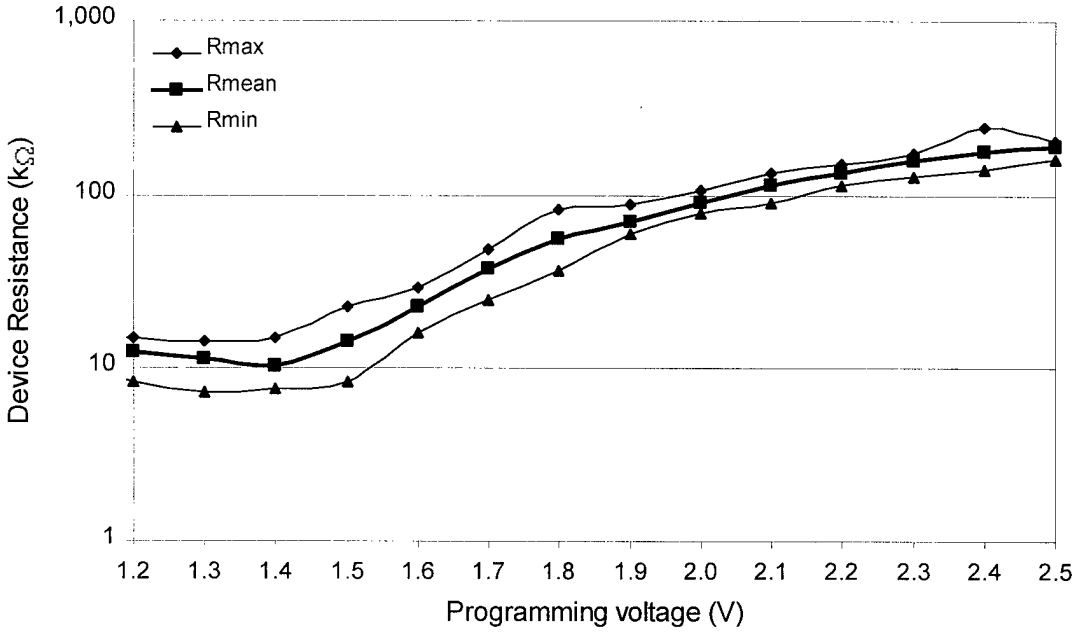


Figure 22. Programming pulse amplitude step increase without reset results

The third device did not demonstrate the same magnitude of the resistance value degradation at the higher characterization repetitions. The device characteristics shown in Figure 24 reveal that most of the step increase without reset repetitions are close in magnitude.

The decrease in the programmed resistance values at the higher repetitions is due to a "memory" affect within the material. When the material is repeatable programmed, poly-crystalline sites, away from the normally formed poly-crystalline filament, are created. These sites represent a "memory" of the last programming event. When the device is programmed to a high resistance state, these sites are not removed from the

material. These sites are not removed because the poly-crystalline sites are located sufficiently far away from the filament that the thermal energy is not supplied long enough to affect them. The only way to remove the sites is to inject thermal energy into the entire device to ensure that all of the material receives enough energy to remove them.

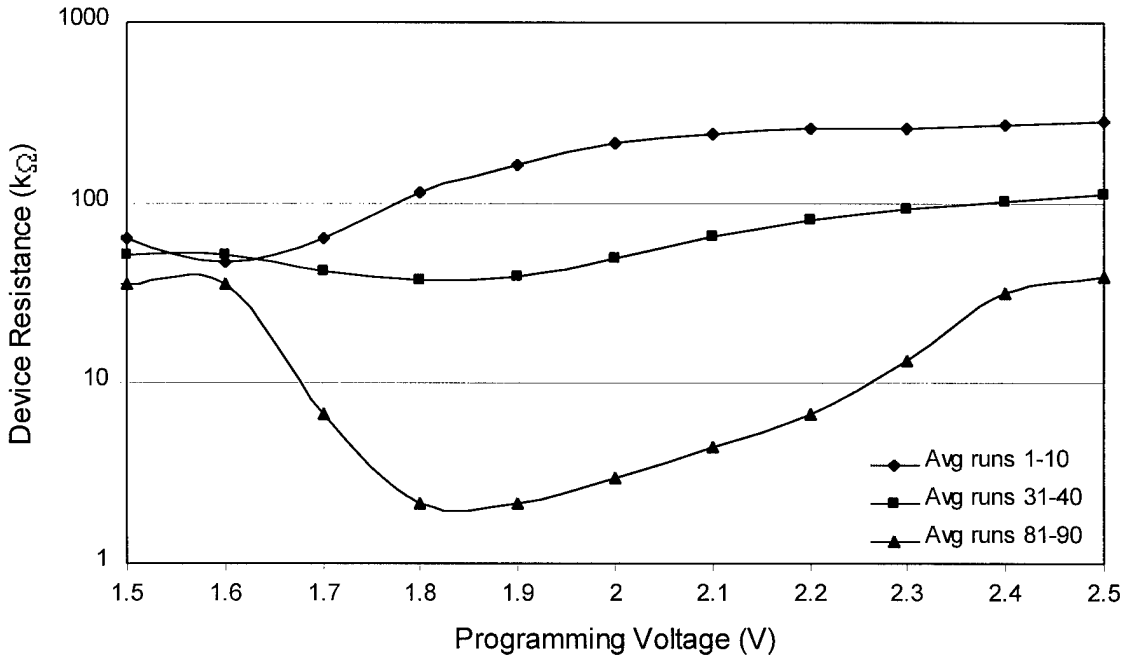


Figure 23. Runs of step increase without reset showing decreasing resistance values

The poly-crystalline sites lead to multiple conduction paths through the material. The multiple paths are very similar to having parallel resistors in the material. Since the resistors are in parallel, the overall resistance of the material is lowered.

Since not every device demonstrated the same magnitude in resistance value degradation, it is likely that the level of degradation is tied to the size of the pore within the device. For devices with a smaller pore size, the energy is supplied along a narrower

channel between the electrodes. Therefore it is less likely that the poly-crystalline sites away from the filament are formed.

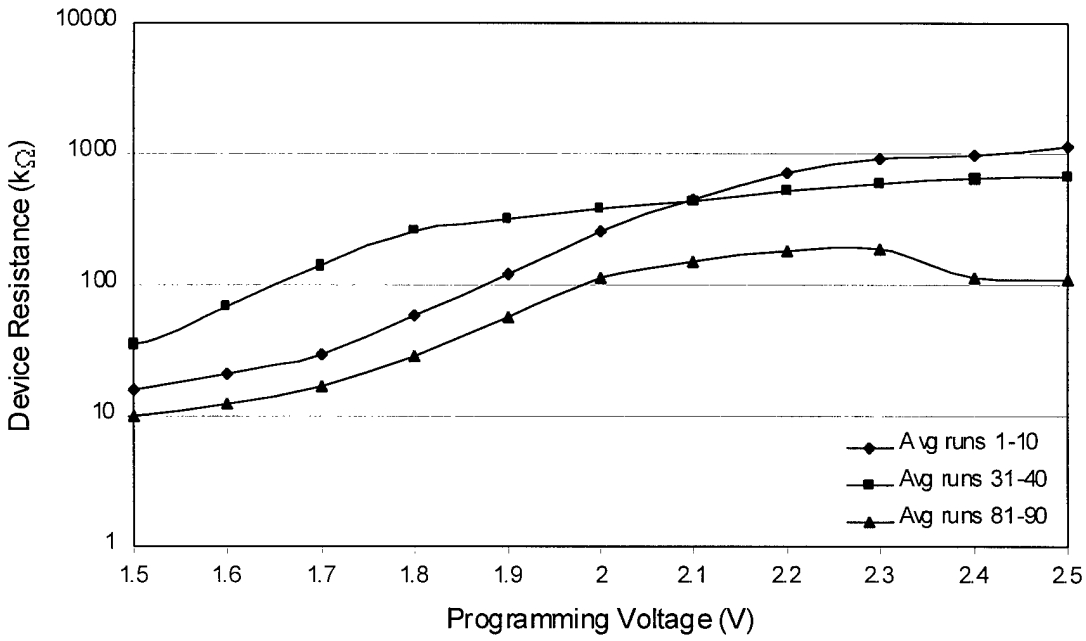


Figure 24. Average runs of the step increase without reset showing less degradation

The programming pulse amplitude step increase with reset characterization expands on the characterization without the reset by resetting the device to a high resistance state between each successive programming pulse. The results of a typical step increase with reset characterization is shown in Figure 25.

Since the step increase with reset characterization returns the device to a high resistance state between each programming, each programming pulse that is higher than the threshold voltage must break the bonds of the amorphous material and realign it to a crystalline state. This is different than the step increase without reset characterization where each applied pulse over the threshold voltage returned parts of the crystalline

filament, formed by the previous programming pulse, back to an amorphous structure. Because each programming pulse must reform the crystalline filament, wider variations in the device resistance for specific programming pulses are expected.

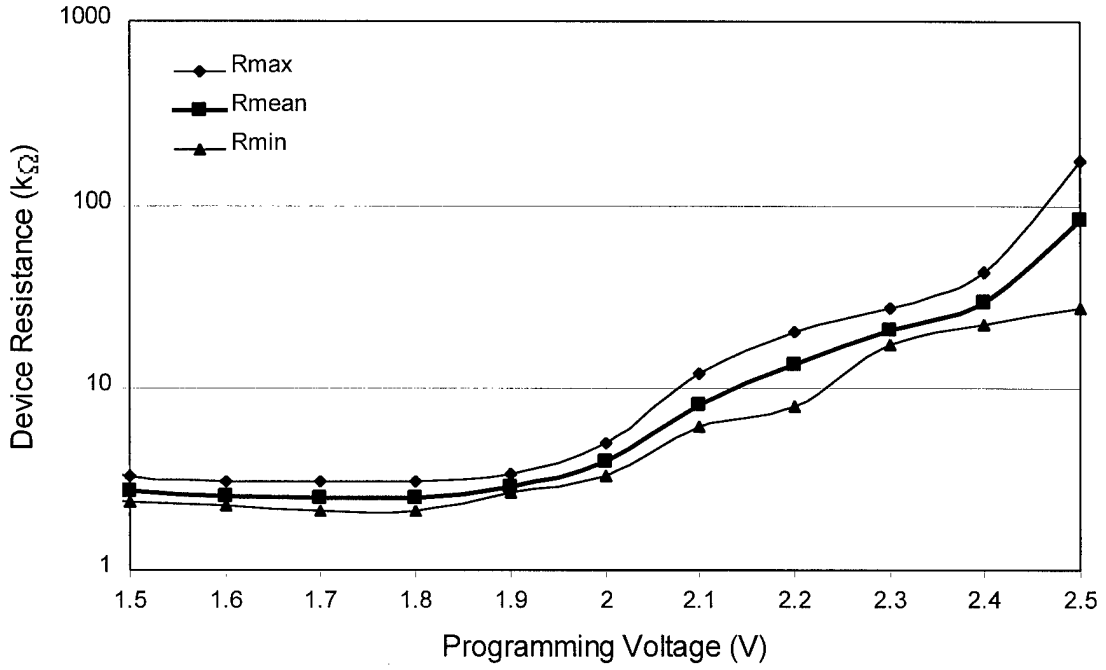


Figure 25. Three runs of the step increase with reset

The repeated step increase with reset programming did produce the repeatable device resistance values as seen in the step increase without reset characterization. However, consistent data values for the step increase with reset were only seen for three consecutive runs at a time, as shown in Figure 25. Figure 26 shows the typical results for more fifteen repeated runs of the with reset characterization. As Figure 26 shows, the resistance values for the programming pulses can vary widely for many runs of this characterization.

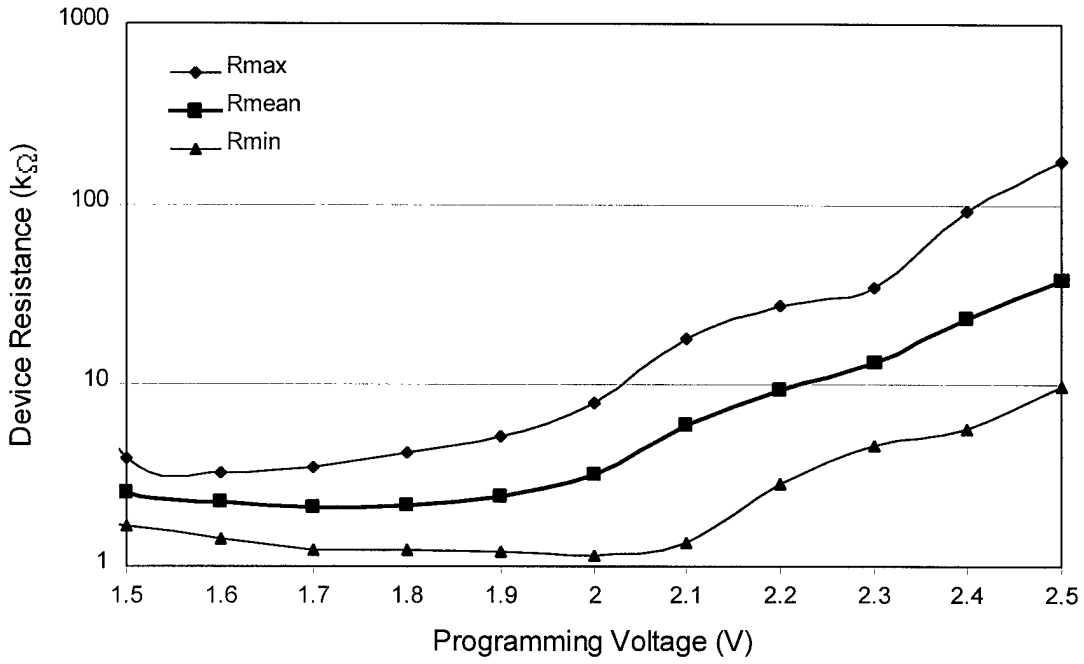


Figure 26. Fifteen runs of the step increase with reset

While some of the variation may be attributed to possible differences in the read voltage described in Appendix A, most of the differences are due to the material itself. Since each programming pulse for the step increase with reset must form a new crystalline filament (since the filament from the previous programming was removed by the reset pulse), there is a high probability that each pulse will not form the exact same filament. Since the filaments differ, the conduction path within the material varies leading to different device resistance values. The variation in the programmed resistance of the material is seen with the larger minimum/maximum values shown in Figure 26.

5.2.2.4 Summary of Repeatability Characterization Results

The results of the repeatability characterizations discussed in this section demonstrated some surprising results. Most of the multiple read characterization results

demonstrated no substantial change in the measured device resistance for the length of the applied reading voltage. However, at several points, the resistance of the device was rapidly reduced and represented an outcome that was not anticipated. The results of the multiple program characterization were expected, with the programming without the reset yielding better results than the characterization with the reset. Most of the results from the programming pulse amplitude step increase characterization were anticipated. Both the step increase with and without reset showed good repeatability over several runs, but the repeatability decrease as the number of runs in increased.

Overall, the results demonstrate that thick film chalcogenide memory devices demonstrate the potential to show the repeatability necessary to be a viable analog memory. Chapter Six discusses the conclusions regarding the overall viability of using the chalcogenide memory devices with regards to repeatability.

5.2.3 Stability Characterization Results

Thick film chalcogenide memory devices must demonstrate stability in order to be used as an accurate analog memory. The primary stability factor examined in this research was device resistance value stability over time. The results presented in this section examines the ability of the thick film chalcogenide memory device to hold a stored resistance value over time.

5.2.3.1 Time Stability

The time characterization examines the ability of the chalcogenide memory device to retain a stored resistance value for specified periods of time. No programming

pulses were applied to the device, therefore, no significant change in the crystallinity of the device should be observed. Because the crystallinity of the device should not change, the measured device resistance value should be constant. The results shown in Table 2 represents a 42 hour test on a thick film chalcogenide memory device. The resistance of the device was measured every half-hour with 15 evenly spaced data points from the 42 hour characterization period selected. Because of the length of the characterization, some anomalous data points were observed. These data points were due to vibrations that caused the probe to temporarily lose contact with the bonding pad of the device resulting in a resistance value that was dramatically out of character with the rest of the data. The anomalous data points were not permanent changes to the crystallinity of the device since subsequent device measurements returned to the expected resistance values. The standard deviation was calculated using equation (10) and treats the data points as a sample of the data population, not the complete population.

Table 2. Typical time characterization results

	Device 1
Rmax (kΩ)	80.54
Rmean (kΩ)	72.33
Rmin (kΩ)	59.64
Std Dev (kΩ)	7.52
Std Dev (% of Mean)	10.40%

5.2.4 Predictability Characterization Results

The predictability of the thick film chalcogenide devices was investigated by comparing the results of the repeatability and stability characterizations for different

memory devices. In addition to these comparisons, an analog resolution of the thick film chalcogenide memory devices was examined by conducting the analog resolution characterization.

5.2.4.1 Repeatability

The chalcogenide memory devices demonstrated some repeatability between devices, usually seen as the same general trend in programmed resistance values. A comparison of the average of ten runs of the programming pulse amplitude step increase characterization without and with reset for two different device is given in Figure 27 and Figure 28. The device resistance values for the individual programming voltages differed drastically at some levels, but the same trend in the resistance values is seen in both devices.

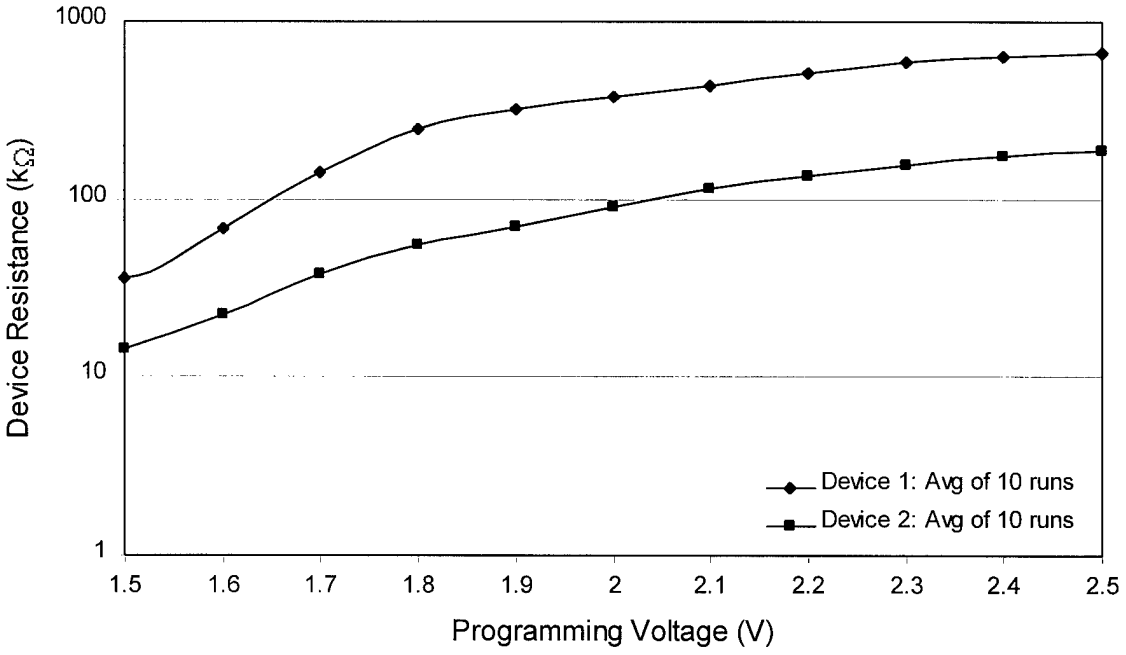


Figure 27. Comparison of the response for two devices for the step increase without reset

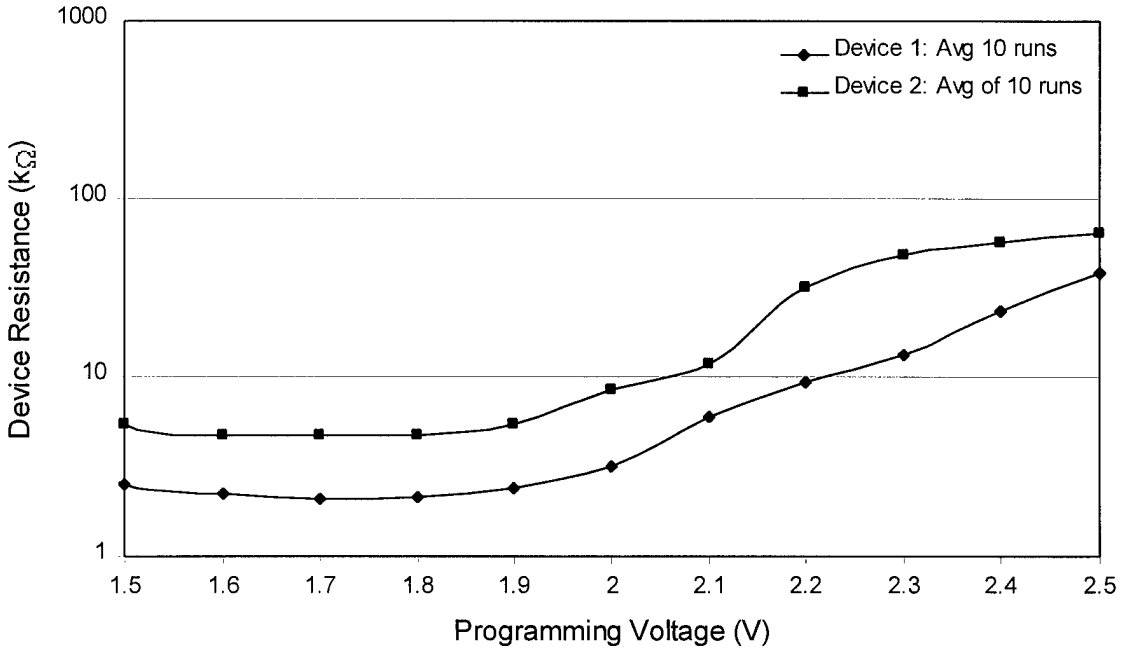


Figure 28. Comparison of two devices for their response to the step increase with reset

5.2.4.2 Stability

The results of the time characterization of two thick film chalcogenide devices are shown in Table 3. The device resistance value for both devices were read every half-hour, with the length of the characterizations taking 42 hours for device 1 and 25 hours for device 2.

Table 3. Comparison of two time characterizations for different devices

	Device 1	Device 2
Rmax (kΩ)	80.54	22.94
Rmean (kΩ)	72.33	21.10
Rmin (kΩ)	59.64	18.51
Std Dev (kΩ)	7.52	1.91
Std Dev (% of Mean)	10.40%	9.06%

Both devices show stability in the device resistance value over time except for a few data points. Data points that are not consistent with the average device resistance values were most likely due to vibration induced measurement problems with the characterization equipment. These problems occurred because the probe made poor contact with the bonding pad of the device, which in turn led to a change in the measured value of the resistance. Additionally, a difference in the voltage across the termination resistor, as described in Appendix A, could also account for some of the differences.

5.2.4.3 Analog Resolution

The analog resolution characterization repeats the step increase without reset characterization, but steps the programming pulse amplitude by the lowest resolution of the pulse generator (0.01V). The results of the average of five analog resolution characterizations for two devices are shown in Figure 29.

The analog resolution characterization demonstrates that the chalcogenide devices have an exponential increase in programmed device resistance for a linear increase in the programming voltage. Although some increases in the programming voltage do not correspond to an increase in the device resistance (as between 1.67V and 1.78V), there are still more than 16 distinguishable levels of resistance values that can be stored and differentiated in the device. The 16 levels correspond to a 4-bit storage capability for the thick film chalcogenide device. However, a smoother increase in resistance value would be desirable. At several locations in both devices, the resistance values are dislocated from the previous value leading to jumps and spikes in the data. These discontinuities arise from a discontinuous rise in the supplied energy from consecutively applied current

pulses. Even though the next programming pulse is slightly higher then the previous pulse, the actual energy delivered is not slightly greater. The accuracy of the programming pulse generator voltage amplitude is ± 1% of the set voltage level [31]. Since the programming amplitude is being increased by just 0.01V, this inaccuracy is enough for subsequent applied voltages to be much greater than 0.01V, or even less than the previous voltage level. This means the energy could be greater than intended or even lower then the previously supplied energy leading to resistance values with jumps and discontinuities, rather than a smooth increase.

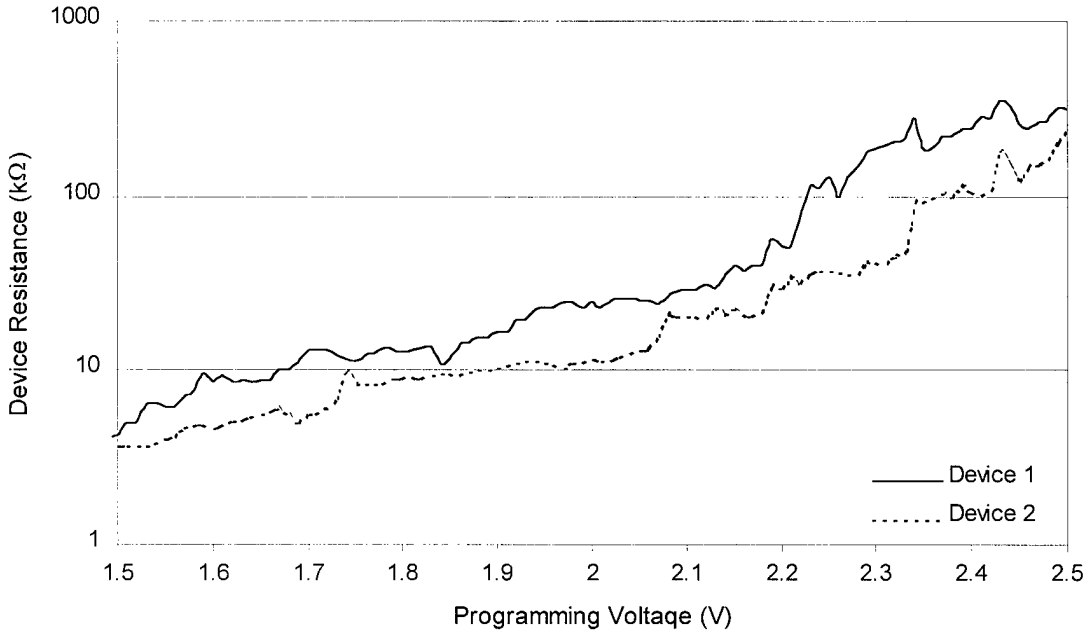


Figure 29. Sample runs of the analog resolution characterization for two devices

5.2.4.4 Summary of Predictability Characterization Results

The chalcogenide devices do demonstrate the same trends in programming for the different repeatability and stability characterizations conducted in this research. However

the actual values of the device resistance for the same repeatability characterizations differ drastically. The stability characterization results were very similar and show strong predictability between the devices. The resolution characterization also shows that the devices have the potential to store at least 4-bit accuracy.

5.3 Summary of Characterization Results

The results of most of the characterizations conducted on the chalcogenide memory devices were expected. The initial parameter characterizations revealed the same programming pulse amplitude and width parameters as the preliminary Ovonyx data. The results of 12 of the 17 multiple read characterizations were as anticipated and did not show any significant change in the resistance value of the device. However, the other five characterizations demonstrated a rapid reduction in the device resistance at an arbitrary point in the characterization, followed by a gradual increase in the device resistance. The reduction and subsequent increase in the resistance value was not expected and is a cause for concern when considering these devices for use as an analog memory device. The outcome of the multiple program characterizations were as expected, with the characterization without the reset having a lower standard deviation than the characterization with the reset. The lower standard deviation between set resistance values for the characterizations without the reset is also seen in the step increase characterization. Additionally, a reduction in resistance values for given programming pulses was seen on two of the devices over the 100 runs of the step increase without reset.

The results of the stability characterization were as expected with the resistance of the device not showing any significant change over time. The outcomes of the predictability characterizations were also as anticipated with different devices demonstrating similar behavior, but differing dramatically in the actual resistance values for identical programming pulses. The analog resolution characterization reveals the potential for better than a 4-bit data storage. Conclusions regarding the fitness of the thick film chalcogenide device for use as an analog memory are discussed in Chapter 6.

6. *Summary and Conclusions*

6.1 Summary of Research

This research examined the validity of using a chalcogenide thin film device as an analog memory. The particular device that was examined is a thick film memory device manufactured by Ovonyx, Inc of Troy, MI. The memory device is nonvolatile and has the ability to be programmed to set resistance levels by applying pulses with a set amplitude and width. The programming pulse supplies the chalcogenide material with thermal energy which breaks the bonds of the material along a filament between the electrodes and allows the material to be set with varying amounts of crystalline and amorphous structure. The amount of crystalline and amorphous structure is set by the amplitude and width parameters of the pulse. Short, high pulses with a rapid trailing edge of less than 3ns break the bonds of the material and quench the material into a highly amorphous state. A longer, lower amplitude pulse with an amplitude greater than the threshold voltage of the device, will break the bonds of the material and will give the atoms of the material enough time to arrange in a low energy, crystalline state. By varying the voltage between the high level of the highly amorphous state and the low level of the highly crystalline state, stable structures between the totally amorphous and crystalline structures can be reached. With a voltage programming range between the threshold voltage and 2.5V and pulse lengths of 100ns for the amorphous state and 200ns for the crystalline state, a device resistance range of 1kΩ to over 1MΩ is achieved.

The viability of using the chalcogenide thick film memory devices as an analog memory was examined by determining if the devices meet the repeatability, stability and predictability properties necessary for an analog memory.

6.2 Conclusions regarding the use of Chalcogenide Devices as an Analog Memory

The results of the characterizations conducted in this research demonstrate a strong potential for the thick film chalcogenide memory device to be used as an accurate analog memory. While the prototype devices characterized in this research are not acceptable for use as a production analog memory, the devices do, at times, exhibit the necessary repeatability, stability and predictability required of an analog memory.

6.2.1 Repeatability

The repeatability characterizations produced mixed results regarding the use of the chalcogenide memory devices as an analog memory. Only the results of the multiple programming without reset measurements demonstrated the level of repeatability required. The multiple read, multiple programming with reset and the programming pulse amplitude step increase characterizations all showed the potential for meeting the requirements for an analog memory, but also demonstrated some undesirable traits that must be mitigated.

Twelve of the seventeen characterization runs of the multiple read characterization produced expected results, while the other five results showed a rapid reduction in the measured resistance of the device. The reduction in the device resistance resulted in both the continuous read and pulsed read characterizations are shown in

Figure 18 and Figure 19 respectively. Since the voltage used to measure the resistance of the device was well below the threshold voltage, the read voltage should not have induced any resistance change within the device. The change in the resistance value observed cannot be adequately explained with only the results shown in this research. Further characterizations must be conducted to pinpoint exactly what is taking place, however, it is likely that thermal energy during the application of the read voltage is causing the formation of micro-crystallites within the material. If these crystallites are formed such that a second conduction path is created between the electrodes, then a switching event may occur. The reduction in the resistance values seen in the multiple read characterizations must be adequately understood and mitigated before the chalcogenide devices can be used as an analog memory.

The results of the multiple program without reset characterization, shown in Figure 20, demonstrated good repeatability of the programming range over the threshold voltage (approximately 1.2V). The low standard deviations indicate that programming a device with identical pulses without resetting shown in Figure 20, will not substantially change the formed crystalline filament and, therefore, does not substantially change the resistance value of the device. However, results of the multiple program with reset characterization, shown in Figure 21, showed much higher standard deviations. The comparison of the multiple program characterization with and without reset demonstrated that the crystalline filament that is formed after each reset can vary widely. Since the filaments formed by the same programming pulse varied, the resistance values of the device can be varied. While some limited variation in the programmed resistance value is acceptable for an analog memory, the level variations shown in would degrade the

performance of the memory to a point where the device would not be practical. To correct the resistance variability caused by a variation in the crystal filament formation, a better design and a tighter control of the fabrication processes is required. The material demonstrates the ability to have a consistent filament formation, as shown in programming voltage 2.4V in Figure 21, however, this level of consistency needs to be extended to reach over the entire programming range. The design of the device needs to be changed to allow a more consistent application of thermal energy from the programming pulse. Only by ensuring that the same energy is supplied to the material for *every* identical programming pulse will consistent filament formation be possible. Additionally, by controlling the fabrication process to a high degree, the consistency necessary for an analog memory should be able to be reached.

The same lack of consistency throughout the programming range was also seen in the step increase characterizations. As with the multiple programming characterization, the step increase characterization without the reset performed better than the characterization with the reset. However, even in the characterization without the reset, some devices demonstrated a substantial lack of consistency. While Figure 24 shows consistent behavior across all 100 runs of the characterization without the reset for a device, Figure 23 shows a degradation as the number of runs increases for a different device. For the characterization with the reset, as shown in Figure 26, the consistency was considerably worse, with the resistance of the device differing by 100kΩ or more for a programming voltage. The potential for more consistent results for both the step increase with and without the reset exists. During portions of both characterizations for every device tested, results were consistent between successive runs. As with the

multiple programming characterizations, material consistency must be increased to yield acceptable results for all of the characterization runs. Again, a better device design and a more tightly controlled fabrication process may also help with the consistency of the programming pulse amplitude step device response.

Overall, the repeatability characterizations clearly illustrate the potential for the chalcogenide memory device to be used as an analog memory. However, to use the devices as an analog memory, the operational consistency that the devices demonstrate over different periods of the characterizations must be improved to cover the entire operating range. The increase in consistency necessary may be achieved by design a device to maximize the consistency supplied during a programming pulse and increasing the quality of fabrication and packaging for the device.

6.2.2 Stability

The results of the stability characterization, shown in Table 2, demonstrate that the programmed resistance values of the chalcogenide memory devices are stable over time. While the time lengths for this research were limited, there is no indication to suggest the resistance values would change given a longer duration of time. Some differences in the resistance value of the device over the time do exist, but can be accounted for by the error induced by the different voltages across the termination resistor, discussed in Appendix A, the device would see over this length of time. The time required to execute this characterization was enough to allow this voltage to drift by more than 0.3mV. For the resistance value of the device given in this characterization, this leads to a difference of up to 20kΩ. The removal of this error leads to resistance

measurements that were much closer to the mean value and would significantly reduce the standard deviation. Given these considerations, the stability of the memory devices should be sufficient for analog memory applications. Therefore, the chalcogenide memory device does demonstrate the time stability required of an analog memory.

6.2.3 Predictability

The chalcogenide memory devices did not demonstrate consistency in the repeatability between the devices acceptable for analog memory applications. However, the devices did demonstrate the potential for the necessary consistency. While the same resistance values were not seen for identical repeatability characterizations, the trend in values, as shown in Figure 27 and Figure 28, was observed to be similar. Since the similar trends for the device resistance values were seen throughout all of the characterizations on the different devices, it is likely that the behavior of the devices will become more predictably with an improved fabrication process. Additionally, the use of a system that provides a standard device area, instead of the first-fire break-through of a silicon nitride layer, should lead to much more consistent results between devices.

The consistency in the time characterization between different devices was very good, with the resistance values of both devices remaining stable. The stability characterization results, shown in Table 3, illustrate the consistency between the devices by showing the resistance values of both devices varying by approximately 10%.

The analog resolution characterization, shown in Figure 29, demonstrated that the devices should be able to provide at least 4-bits of resolution. However, to achieve better analog precision, and thus a better analog performance, the jumps and

discontinuities seen in Figure 29 must be removed by redesigning the device to have a more reliable way to apply small changes in supplied energy.

6.2.4 Comparison to Current Analog Memories

A functional thick-film chalcogenide memory device (one which demonstrated the consistent behavior) would have all of the benefits of the current analog memories discussed in section 2.3.2, but would not have the drawbacks. The chalcogenide devices, unlike the floating-gate and charge-trapping memories, require low programming voltages (<2.5V). Additionally, the programming voltages of the chalcogenide devices are scalable, so as the device size decreases, the programming voltages also decrease [34]. The programming times of the chalcogenide devices (200ns) are also much faster than the floating-gate and charge-trapping memories (>1ms). The chalcogenide material is easily integrated with current VLSI CMOS fabrication processes. Programming chalcogenide devices is a simple voltage controlled process that needs only positive voltages. Finally, the chalcogenide memory devices can be used in simple circuits that minimize the amount of additional support circuits for a uncomplicated, easy to use design.

An additional benefit of the chalcogenide memory devices is its inherent nonvolatility. Nonvolatility is not a requirement for analog data storage, its inclusion greatly increases the flexibility of the devices. Not only can the chalcogenide memory devices be used to store analog data values, but they can be used to retain those values over time without applied power.

6.2.5 Summary of Conclusions

Characterization results do not indicate any insurmountable reasons why the thick film chalcogenide memory device could not be used as an analog memory. All of the devices characterized in this research illustrated behavior that would be acceptable for meeting the requirements of an analog memory. However, the devices did not consistently exhibit acceptable behavior. The results show that through further refinement of the devices and an improved fabrication process, the potential exists to make the desired operation of the devices more consistent. Additionally, refinement of the devices and the improvement in the fabrication process may lead to an increase in the consistency between the devices. An increase in the device consistency will improve repeatability and predictability as required for an analog memory.

Reduction in the stored resistance value during the multiple read characterizations should be explored further. This phenomena must be sufficiently understood and mitigated before the device can be used as an analog memory.

An increase in the consistency of the repeatability and predictability will make the thick film chalcogenide memory device a desirable analog memory. The desirability of the thick film chalcogenide device is increased when considering the low programming voltages, fast programming and reading times, and non-volatility that the device also exhibits. However, before the device can be used to accurately and repeatably store analog data, improvements must be made.

6.3 Lessons Learned

The characterization of the thin film and the thick film chalcogenide memory devices revealed numerous challenges, from both the device and the characterization equipment.

6.3.1 Electrostatic Discharge

The chalcogenide memory devices are very susceptible to electrostatic discharge (ESD). ESD can provide a voltage with enough thermal energy to have unwanted changes in the resistance values stored in chalcogenide memory devices. ESD also has the potential to permanently damage chalcogenide devices. The memory devices must be handled properly to prevent ESD from becoming a problem. During the initial characterization equipment set-up, the thin film chalcogenide memory devices were not handled properly and all of the devices bonded to the output pins of the chip were damaged by ESD. Devices damaged by ESD show an extremely low resistance measurement, usually around 100Ω or less.

6.3.2 Characterization Equipment

The equipment used to characterize the chalcogenide needs to be free of any type of spurious outputs. A voltage spike upon the reset of a piece of equipment could be coupled into the device, possibly causing a change in the device resistance or permanent damage to the device. These spurious voltages can act very much like the ESD discussing in section 6.3.1.

6.3.3 Higher Programming Voltage Amplitudes

Programming the device with a programming voltage higher than 2.5V will lead to degraded performance in the device. The use of the higher voltage leads to the high resistance saturation voltage moving from 2.5V to over 4.0V. Once higher voltages are used, the programming voltage range (now V_{th}-4.0V) permanently shifts and comparisons of resistance values to the previous voltage range (V_{th}-2.5V) cannot be made.

6.4 Recommendations for Future Research

Additional characterizations must be conducted on the devices to determine the reason for the reduction in the resistance values seen in the later runs of the multiple read characterizations. The additional characterizations should determine whether the reduction in the resistance value is due to the characterization equipment or the material itself.

The characterization of the thick film chalcogenide devices can be taken a step further to investigate the affects that different temperatures and radiation levels have on both device programming and data retention. Chalcogenide memory devices have already shown a considerable sensitivity to temperature changes [2]. This temperature sensitivity is not surprising considering that thermal energy is responsible for bond breaking and crystallization. Since heating a device will supply energy to the material, it would be expected that the material will become more amorphous. The increase in amorphous structure is due to energy breaking the weak bonds of any crystalline filaments, causing the device to move into a higher amorphous state [19].

Chalcogenide devices should demonstrate a radiation hardness to total ionizing dose radiation, but may be susceptible to high-energy ion strikes. Since operating chalcogenide devices does not depend on an electric field, any charge trapped in the oxides of the device will not affect the device performance. However, a single, high-energy ion that strikes a device may impart enough energy to break some of the bonds in the device, returning some of the crystalline material to an amorphous state. If the ion does cause bond breaking within the device, then the potential exists for a change in the stored resistance value of the device.

Appendix A. Error Source in Characterizations

A significant source of error was revealed when the initial characterization was conducted on the thin film memory devices. The circuit in Figure 13 does not always correspond to the resistance equation in equation (9) because of real world factors such as electromagnetic interference. These factors shift the voltage across the termination resistor, R_T, enough to alter the results of some of the characterizations by 50%. This error is more dramatic at higher resistance levels because the voltage across the device, V_D, is close to the voltage across the resistance R_T. The closer the voltage values across R_T and the device, the smaller the denominator in equation (9) and the larger the value of the device resistance. If the voltage across R_T changes, then the difference in the voltage across R_T and the voltage across the device will be smaller or larger, and can significantly affect any results of equation (9). However, the voltage across R_T changes very slowly and the results of any characterization that completes within a few minutes will see essentially the same voltage across R_T. Therefore, the results of short characterizations will not have much error due to the shift in the voltage. Characterizations that compare device resistance values from characterizations that are more than 5 minutes apart are very susceptible to resistance difference due only to a difference in the voltage across R_T. Equation (9) also had to be modified to account for the difference in the resistor values. Without this change, the equation (9) would yield negative values for the resistance of the device since the voltage across the device could be greater then the reference voltage in the denominator. The change to the equation consisted of increasing the reference

voltage in the dominator to match the largest open circuit voltage the circuit in Figure 13 sees as measured with the HP 3485. From observation, this reference value was determined to be 0.10379V. This leads equation (9) to be modified to:

$$R_D = \frac{1025 \cdot V_D}{0.10379 - V_D}(\Omega) \tag{11}$$

The source of error in the characterization of the chalcogenide devices can be removed by adding another multimeter to the circuit in Figure 13. By recording the voltage across the termination resistor for each device resistance reading, a more accurate measurement can be made by using the voltage read from the added multimeter as the reference voltage in the denominator of equation (10). The addition of the second multimeter creates the following characterization circuit shown in Figure 30 and the new device resistance equation:

$$R_D = \frac{1025 \cdot V_D}{V_R - V_D}(\Omega) \tag{12}$$

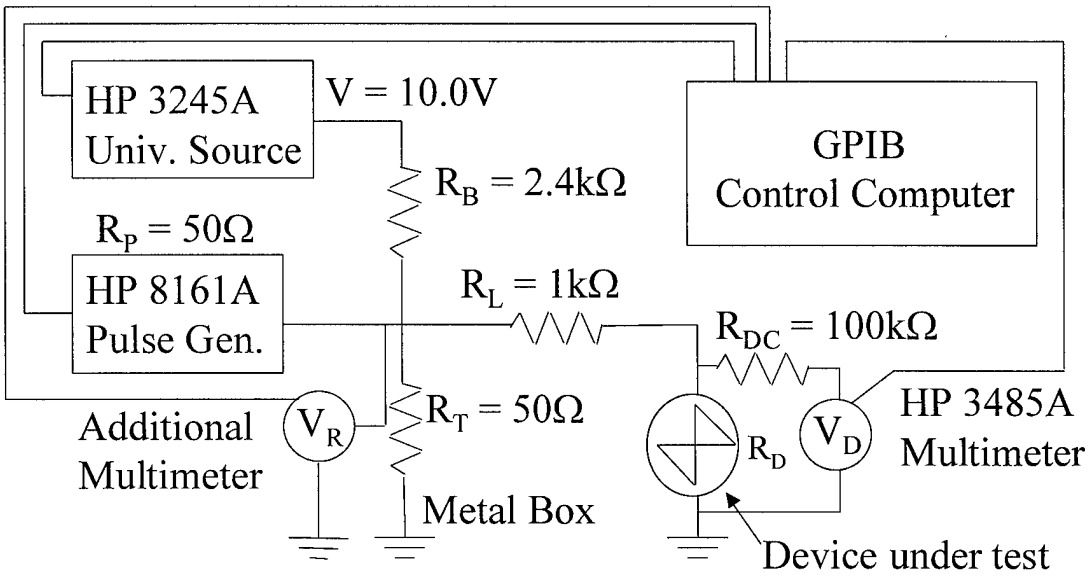


Figure 30. Future Research Characterization Circuit

References

1. Murray, A. F. and Buchan L.W., "A User's Guide to Non-Volatile, On-Chip Analogue Memory," *Electronics & Communication Engineering Journal,* April 1998, pp. 53-63

2. Lowery, T., "Ovonic Unified Memory," ECD Presentation, http://ovonic.com/website_OUM.pdf

3. Ovshinsky, S. R., "An Introduction to Ovonic Research," *Journal of Non-Crystalline Solids,* Vol. 2, 1970, pp. 99-106

4. Adler, D., "Theory gives shape to amorphous materials," *Electronics*, Vol. 43, No. 20 ,28 Sep 1970, pp. 61-72

5. Ovshinsky, S., R., "Amorphous Materials-Past, Present and Future," *Journal of Non-Crystalline Solids,* Vol. 73, 1985, pp. 395-408

6. Nagels, P. "Electronic Transport in Amorphous Semiconductors," *Topics in Applied Physics: Amorphous Semiconductors*, Brodsky, M. H. (ed.), 2nd Edition, Springer-Verlag, 1985

7. Herms, W., "Defects and Threshold Switching in Chalcogenides," *International Journal of Electronics*, Vol. 73, No. 5, 1992, pp. 907-910

8. Street, R. A. and Mott, N. F., "States in the Gap on Glassy Semiconductors," *Physical Review Letters,* Vol. 35, Num. 19, 10 Nov 1975, pp. 1293-1296

9. Kastner, M., Adler, D., and Fritzsche, H., "Valence-Alternation Model for Localized Gap States in Lone-Pair Semiconductors," *Physical Review Letters,* Vol. 37, Num. 22, 29 Nov 1976, pp. 1504-1507

10. Emin, D. "Aspects of the Theory of Small Polarons in Disordered Materials," *Electronic and Structural Properties of Amorphous Semiconductors,* Le Comber, P. G. and Mort, J. (ed.), Academic Press, 1973

11. Emin, D. "Small-Polaron Model of the Low-Temperature Optically Induced Properties of Chalcogenide Glasses," *Amorphous and Liquid Semiconductors,* Spear, W. E. (ed.), Proceedings of the Seventh International Conference on Amorphous and Liquid Semiconductors, 1977

12. Hajto, J., Owen, A. E., Snell, A. J., LeEcomber, P. G., and Rose, M. J., "Electronic Switching in Amorphous Semiconductor Thin Films, "*Amorphous & Microcrystalline Semiconductor Devices, Vol. II: Materials and Device Physics,* Kanicki, J., Ed., Artech House, 1992, pp. 641-701

13. Palmer, R. G., Stein, D. L., Abrahams E., and Anderson, P. W., "Models of Hierarchically Constrained Dynamics for Glassy Relaxation," *Physical Review Letters*, Vol. 53, No. 10, 3 Sep 1984, pp. 958-961

14. Ovshinsky, S. R., "Fundamentals of Amorphous Semiconductors," *Physical Properties of Amorphous Materials*, Plenum Press, New York, 1985, pp. 105-155

15. Ovshinsky, S. R., "The Ovshinsky Switch," *Proceedings of the Fifth Annual National Conference on Industrial Research,* Chicago, Ill., 18-19 Sep 1969, pp. 86-90

16. Ovshinsky, S. R. and Fritzsche, H., "Amorphous Semiconductors for Switching, Memory and Imaging Applications," *IEEE Transactions on Electron Devices,* Vol. ED-20, No. 2, Feb 1973, pp. 91-105

17. Shaw, M. P., "Switching and Memory Effects in Thin Amorphous Chalcogenide Films – Thermophonic Studies," *Disorder and Order in the Solid State,* Pryor R. W., Schwartz B. B., Ovshinsky S. R., Ed., Plenum Press, New York, 1988, pp. 53-66

18. Neale, R. G., Nelson, D. L., and Moore, G. E., "Nonvolatile and reprogrammable, the read-mostly memory is here," *Electronics*, Vol. 43, No. 20, 28 Sep 70, pp. 56-60

19. Ovonyx Inc, Chalcogenide memory experimental data, 20 Aug 1999

20. "Analog Systems Summary," *Anava Corp.* http://www.anava.com/analog.html

21. Patterson, D. A. and Hennessy J. L., *Computer Organization and Design*

22. Brown, W. D. and Brewer, J. E., *Nonvolatile Semiconductor Memory,* IEEE Press, 1998

23. Sharma, A. K. *Semiconductor Memories,* IEEE Press, 1997

24. Neaman, D. A., *Semiconductor Physics & Devices*, McGraw-Hill, 2nd Ed, 1997

25. Zucher, P., Jones, R. E., Chu, P. Y., Taylor, D. J., White Jr., B. E., Zafar, S., Jiang, B., Lii, Y. T., and Gillespie, J., "Ferroelectric Nonvolatile Memory Technology: Applications and Integration Challenges," *IEEE Transactions on Components, Packing, and Manufacturing Technology—Part A*, Vol. 20, No. 2, June 1997

26. Rose, M. J., Snell, A. J., LeEcomber, P. G., Hajto, J., Fitzgerald, A. G., and Owen, A. E., "Aspects of Nonvolatility in a-Si-H memory Devices," *Amorphous Silicon Technology*, 1992, 258, pp. 1075-1080

27. Reeder, A. A., Thomas, I. P., Smith, C., Wittgreffe, J., Godfrey, D. J., Hajto, J., Owen, A. E., Snell, A. J., Murray, A. F., Rose, M. J., Osbourne, I. S., and LeEcomber, P. G., "Application of Analogue a-Si Memory Devices to Resistive Synapses for Neural Networks," *Proc. Materials Research Society Symposium*, 1992, 258, pp. 1081-1086

28. Ovonyx Inc., 1675 West Maple Road, Troy, MI. 48084

29. Bernacki, S., Hunt, K., Tyson, S., Hudgens, S., Pashmakov, B., Czubatyj, W., and Spall, E., "Total Dose Radiation Hardness and High Temperature Imprint Characteristics of C-RAM Resistor Elements," Unpublished.

30. LabVIEW, http://www.ni.com

31. *HP 8131A 500MHz Pulse Generator: Operating and Programming Manual*, Hewlett-Packard Co., Ed 1, Jul 1989

32. *HP 3245A Universal Source: Operating and Programming Manual*, Hewlett-Packard Co., Ed 1, Sep 1988

33. *HP 3485 Multimeter: Operating, Programming and Configuration Manual*, Hewlett-Packard Co., Ed 1, May 1988

34. ECD, Inc., *New Nonvolatile Memory Technology*, AFRL presentation provided by Dr. H. Schöne

Vita

Captain Travis F. Blake was born on 10 October 1973 in Würzberg, West Germany. He graduated from Lake Braddock Secondary School, Burke, Virginia, in 1991. Upon accepting an Air Force ROTC scholarship, he attended the Georgia Institute of Technology, graduating in June 1995 with a Bachelor of Computer Engineering degree. Upon graduation he was commissioned as a Second Lieutenant in the United States Air Force and designated a Distinguished Graduate from AFROTC Detachment 165. His reserve officer commission was upgraded to a regular commission in 1996.

Captain Blake's first assignment was as an electrical engineer in the 5th Space Launch Squadron, 45th Space Wing, Cape Canaveral Air Station, Florida. Captain Blake directly participated in four successful Titan IVA/B launches as both an Upperstage and Facility Engineer and an Air Force Facility Officer. After two years in the launch squadron, he was transferred to the 45th Space Wing Command Post, Patrick AFB, Florida. As the Operations Officer for the Command Post, Captain Blake participated in every aspect of command and control and emergency operations for the 45th Space Wing. In 1999, Captain Blake was selected to attend the Graduate School of Engineering, Air Force Institute of Technology (AFIT) to begin study for a Master of Science Degree in Electrical Engineering. He graduated from AFIT on 21 March 2000.

REPORT DOCUMENTATION PAGE	Form Approved OMB No. 074-0188

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	March 2000	Master's Thesis

4. TITLE AND SUBTITLE

Investigation of $Ge_2Te_2Sb_5$ Chalcogenide Films for Use as an Analog Memory

5. FUNDING NUMBERS

6. AUTHOR(S)

Travis F. Blake, Captain, USAF

7. PERFORMING ORGANIZATION NAMES(S) AND ADDRESS(S)

Air Force Institute of Technology
Graduate School of Engineering and Management (AFIT/EN)
2950 P Street, Building 640
WPAFB OH 45433-7765

8. PERFORMING ORGANIZATION REPORT NUMBER

AFIT/GE/ENG/00M-04

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)

AFRL/VSSE
Attn: Dr. Robert Pugh
3550 Aberdeen Ave. S.E.
Kirtland AFB, NM 87117-5776 DSN: 246-0585

10. SPONSORING / MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

Maj Charles P. Brothers, Jr., Ph.D. , ENG, DSN: 785-3636, ext. 4618

12a. DISTRIBUTION / AVAILABILITY STATEMENT

APPROVED FOR PUBLIC RELEASE; DISTRIBUTION UNLIMITED.

12b. DISTRIBUTION CODE

ABSTRACT (*Maximum 200 Words*)

This work investigates the feasibility of using $Ge_2Te_2Sb_5$ chalcogenide films for analog memory. Thick film chalcogenide memory devices provided by Ovonyx, Inc. are characterized to determine how well the devices meet the repeatability, stability and predictability criteria needed to accurately store analog data values. Chalcogenide memory devices take advantage of the phase-shifting nature of chalcogenide materials to store the analog data as a resistance level.

An automated test system was developed to characterize the material and the prototype devices with the goal to determine the 1) non-destructive readability of the device at different resistance values; 2) repeatability of programming the device; 3) stability the resistance value has over time; 4) parametric variations between devices; and 5) maximum and reliably achievable analog resolution.

The results of these characterizations demonstrate that thick film chalcogenide devices possess the necessary repeatability, stability and predictability properties needed in an analog memory, with at least a 4-bit analog resolution. However, the prototype devices, as produced for this research, do not demonstrate these properties consistently. A full scale, commercial fabrication process is likely to improve the device design and manufacture so it can be used as an analog memory.

14. SUBJECT TERMS	15. NUMBER OF PAGES
Chalcogenide material, $Ge_2Te_2Sb_5$, amorphous semiconductors, noncrystalline solids, analog memory	123
	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL